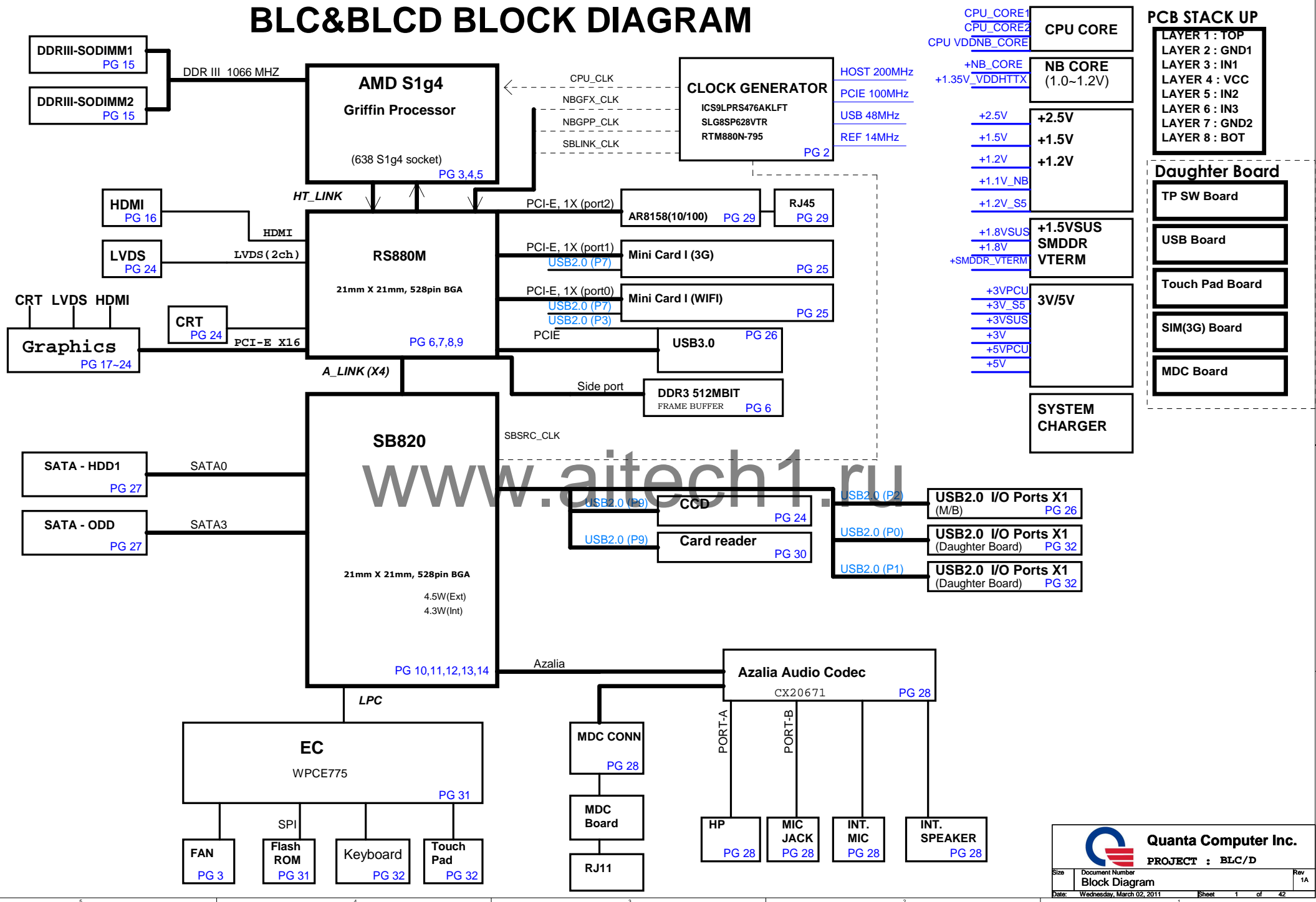
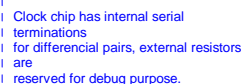
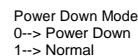
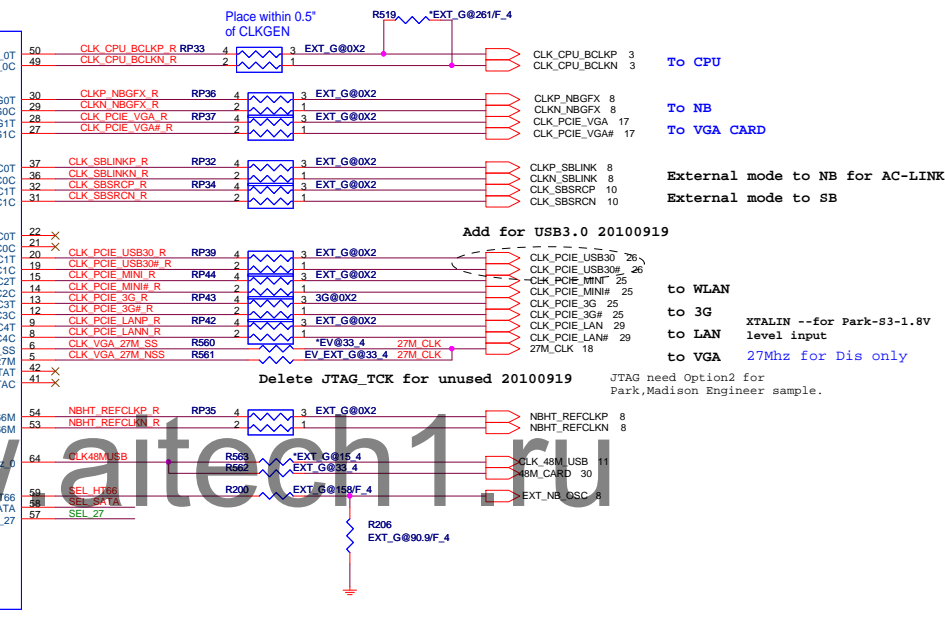
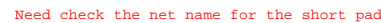
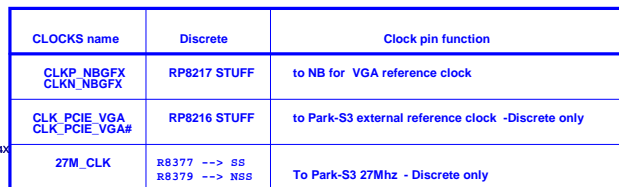


# BLC&BLCD BLOCK DIAGRAM



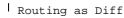
## 02



* default		
SEL_HTT66 (HTT)	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA (SR6)	1	100 MHz non-spreading differential SRC clock
	0*	100 MHz spreading differential SRC clock
SEL_27 (SR7)	1*	27MHz non-spreading single clock
	0	100 MHz spreading differential SRC clock



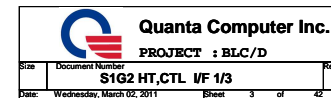
Keep trace from resisor to CPU within 0.6"  
keep trace from caps to CPU within 1.2"

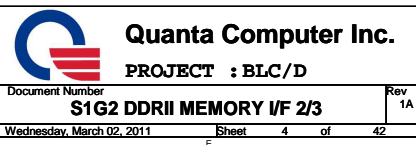


If no sideband support  
(R368,R373,Q27,R656 let as NC)

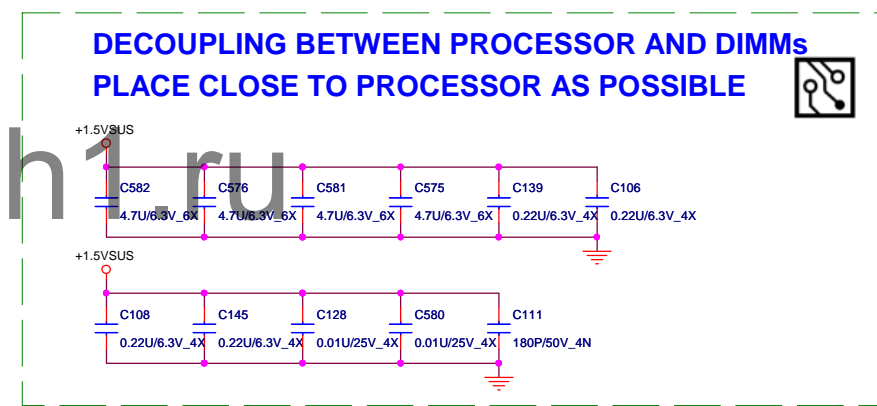
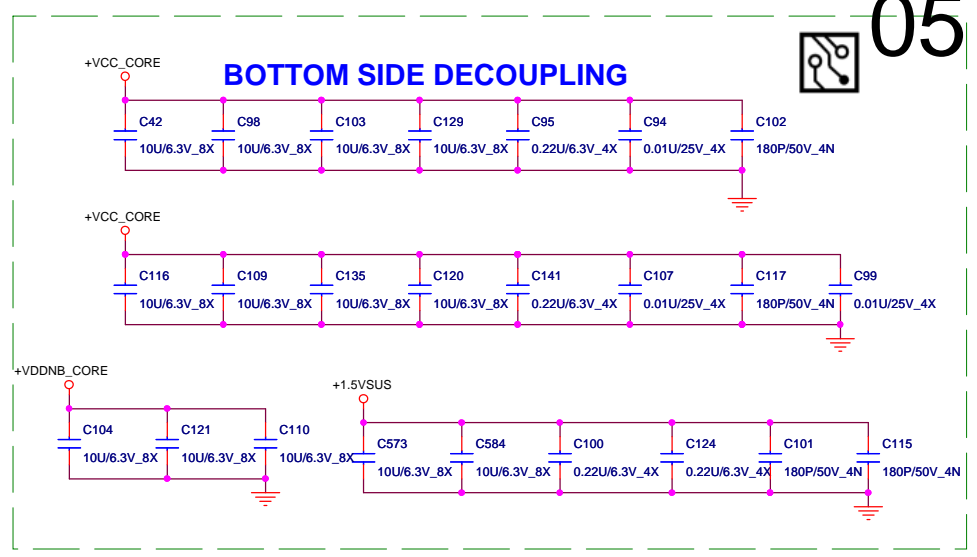
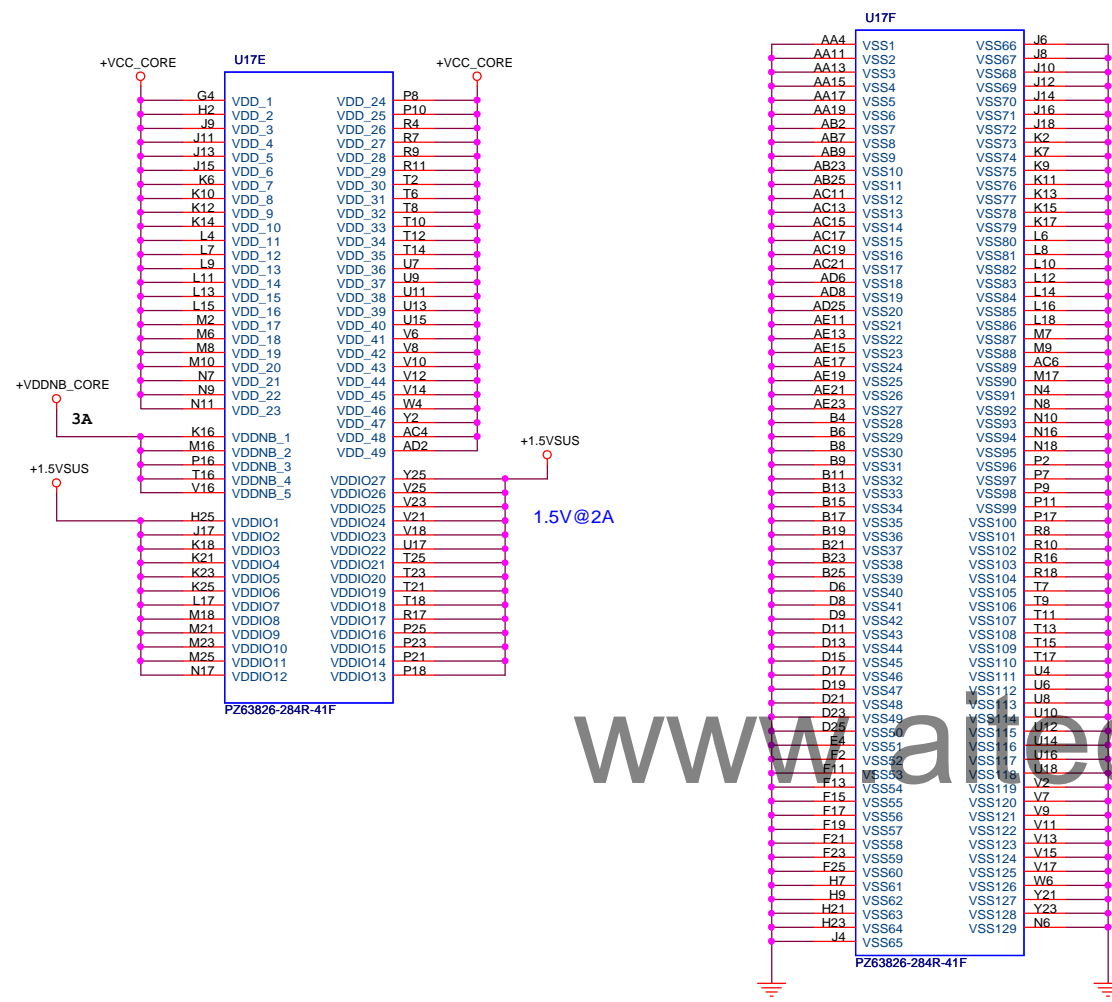


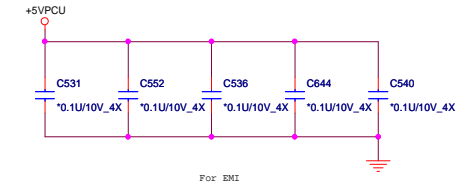
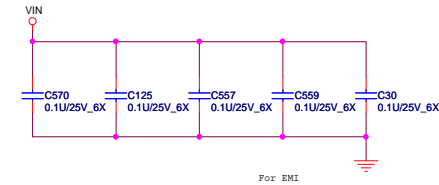
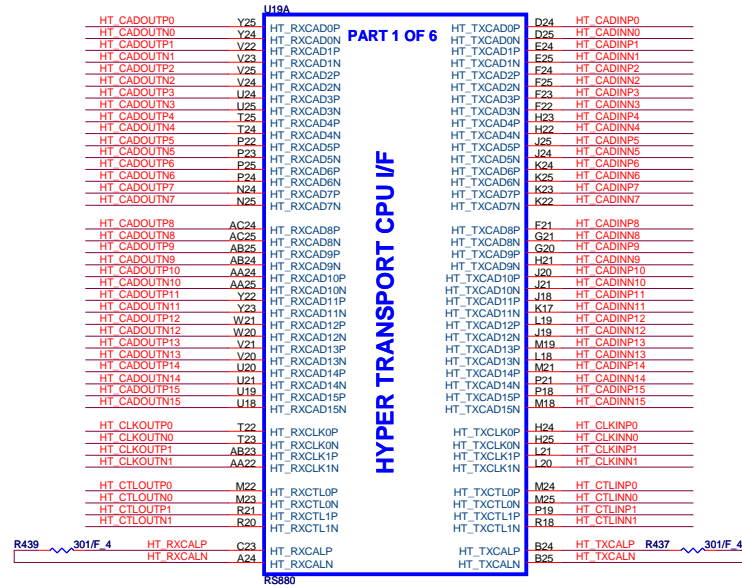
### VID Override Circuit

CPU FAN

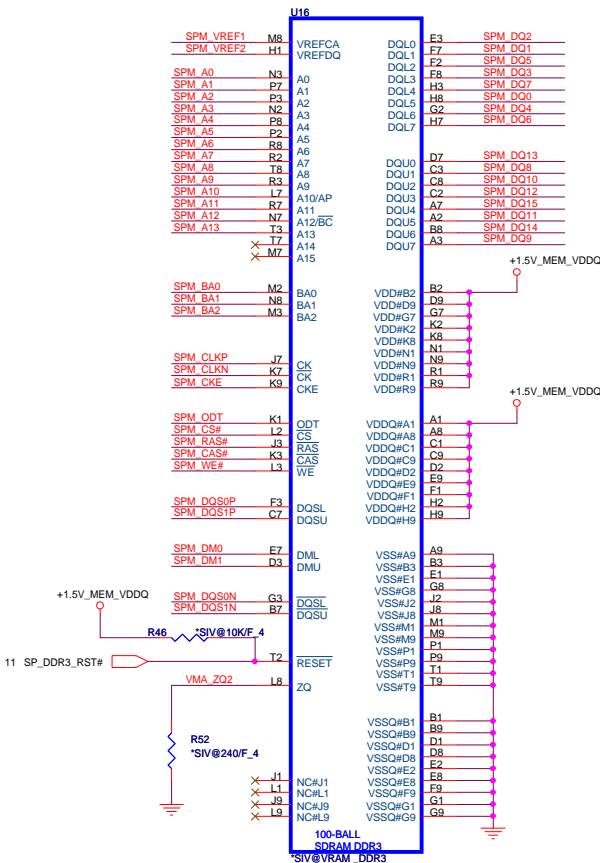






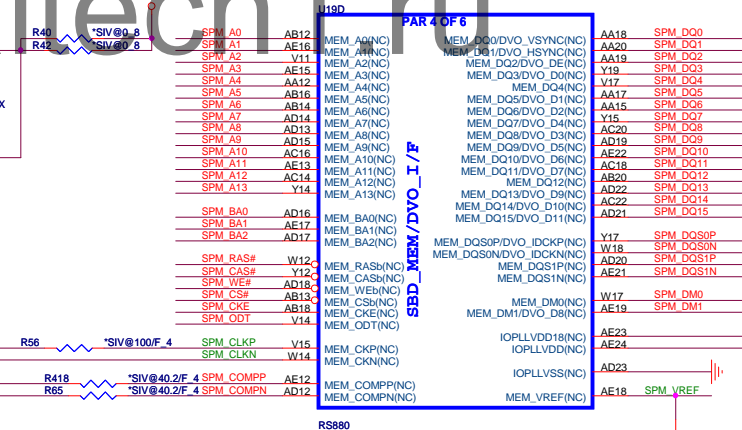
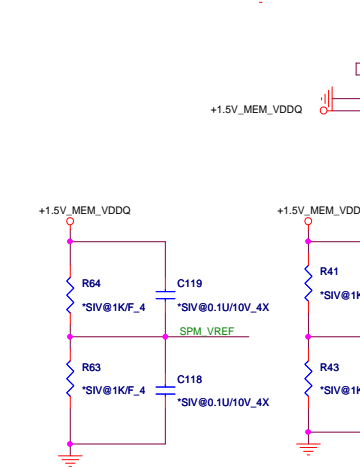
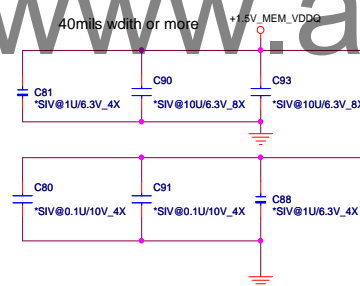


## Memory Side Port



This block is for UMA only . Discrete can remove all component

www.aitech1.ru



Quanta Computer Inc.

PROJECT : BLC/D

## PART 2 OF 6

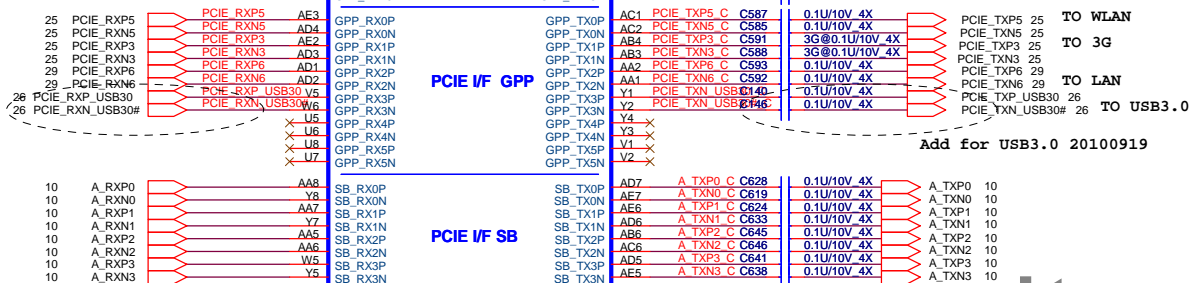
## PCIE I/F GFX

PEG_RXP15	D4	GFX_RX0P
PEG_RXN15	C4	GFX_RX0N
PEG_RXP14	A3	GFX_RX1P
PEG_RXN14	B3	GFX_RX1N
PEG_RXP13	C2	GFX_RX2P
PEG_RXN13	C1	GFX_RX2N
PEG_RXP12	E5	GFX_RX3P
PEG_RXN12	F5	GFX_RX3N
PEG_RXP11	G5	GFX_RX4P
PEG_RXN11	G6	GFX_RX4N
PEG_RXP10	H6	GFX_RX5P
PEG_RXN10	H6	GFX_RX5N
PEG_RXP9	J6	GFX_RX6P
PEG_RXN9	J5	GFX_RX6N
PEG_RXP8	J7	GFX_RX7P
PEG_RXN8	J8	GFX_RX7N
PEG_RXP7	L6	GFX_RX8P
PEG_RXN7	L6	GFX_RX8N
PEG_RXP6	M8	GFX_RX9P
PEG_RXN6	L8	GFX_RX9N
PEG_RXP5	P7	GFX_RX10P
PEG_RXN5	M7	GFX_RX10N
PEG_RXP4	P5	GFX_RX11P
PEG_RXN4	M5	GFX_RX11N
PEG_RXP3	R8	GFX_RX12P
PEG_RXN3	P8	GFX_RX12N
PEG_RXP2	R6	GFX_RX13P
PEG_RXN2	R5	GFX_RX13N
PEG_RXP1	P4	GFX_RX14P
PEG_RXN1	P3	GFX_RX14N
PEG_RXP0	T4	GFX_RX15P
PEG_RXN0	T3	GFX_RX15N

A5	C	PEG_TXP15	C612	EV@0.1U/10V_4X	PEG_TXP15
B5	C	PEG_TXN15	C617	EV@0.1U/10V_4X	PEG_TXN15
A4	C	PEG_TXP14	C636	EV@0.1U/10V_4X	PEG_TXP14
B4	C	PEG_TXN14	C635	EV@0.1U/10V_4X	PEG_TXN14
C3	C	PEG_TXP13	C632	EV@0.1U/10V_4X	PEG_TXP13
B2	C	PEG_TXN13	C631	EV@0.1U/10V_4X	PEG_TXN13
D1	C	PEG_TXP12	C643	EV@0.1U/10V_4X	PEG_TXP12
D2	C	PEG_TXN12	C642	EV@0.1U/10V_4X	PEG_TXN12
E2	C	PEG_TXP11	C723	EV@0.1U/10V_4X	PEG_TXP11
F1	C	PEG_TXN11	C725	EV@0.1U/10V_4X	PEG_TXN11
F4	C	PEG_TXP10	C727	EV@0.1U/10V_4X	PEG_TXP10
F3	C	PEG_TXN10	C729	EV@0.1U/10V_4X	PEG_TXN10
F1	C	PEG_TXP9	C731	EV@0.1U/10V_4X	PEG_TXP9
F2	C	PEG_TXN9	C733	EV@0.1U/10V_4X	PEG_TXN9
H4	C	PEG_TXP8	C734	EV@0.1U/10V_4X	PEG_TXP8
H3	C	PEG_TXN8	C735	EV@0.1U/10V_4X	PEG_TXN8
H1	C	PEG_TXP7	C737	EV@0.1U/10V_4X	PEG_TXP7
H2	C	PEG_TXN7	C739	EV@0.1U/10V_4X	PEG_TXN7
J2	C	PEG_TXP6	C741	EV@0.1U/10V_4X	PEG_TXP6
J1	C	PEG_TXN6	C742	EV@0.1U/10V_4X	PEG_TXN6
K4	C	PEG_TXP5	C743	EV@0.1U/10V_4X	PEG_TXP5
K3	C	PEG_TXN5	C745	EV@0.1U/10V_4X	PEG_TXN5
K1	C	PEG_TXP4	C746	EV@0.1U/10V_4X	PEG_TXP4
K2	C	PEG_TXN4	C749	EV@0.1U/10V_4X	PEG_TXN4
M4	C	PEG_TXP3	C750	EV@0.1U/10V_4X	PEG_TXP3
M3	C	PEG_TXN3	C755	EV@0.1U/10V_4X	PEG_TXN3
M1	C	PEG_TXP2	C757	EV@0.1U/10V_4X	PEG_TXP2
M2	C	PEG_TXN2	C760	EV@0.1U/10V_4X	PEG_TXN2
N2	C	PEG_TXP1	C761	EV@0.1U/10V_4X	PEG_TXP1
N1	C	PEG_TXN1	C763	EV@0.1U/10V_4X	PEG_TXN1
P1	C	PEG_TXP0	C765	EV@0.1U/10V_4X	PEG_TXP0
P2	C	PEG_TXN0	C767	EV@0.1U/10V_4X	PEG_TXN0

PEG_TXN[15:0]	PEG_TXN[15:0]	17
PEG_TXP[15:0]	PEG_TXP[15:0]	17
PEG_RXN[15:0]	PEG_RXN[15:0]	17
PEG_RXP[15:0]	PEG_RXP[15:0]	17

LAN Reverse by soft strap



Add for USB3.0 20100919

## PCIE I/F SB

PCE\_CALRP(PCE\_BCALRP)  
PCE\_CALRN(PCE\_BCALRN)

RS880

## NOTE:

RS880MC no support Graphic / HDMI / DP

## UMA ONLY

Close to North Bridge

Close to North Bridge

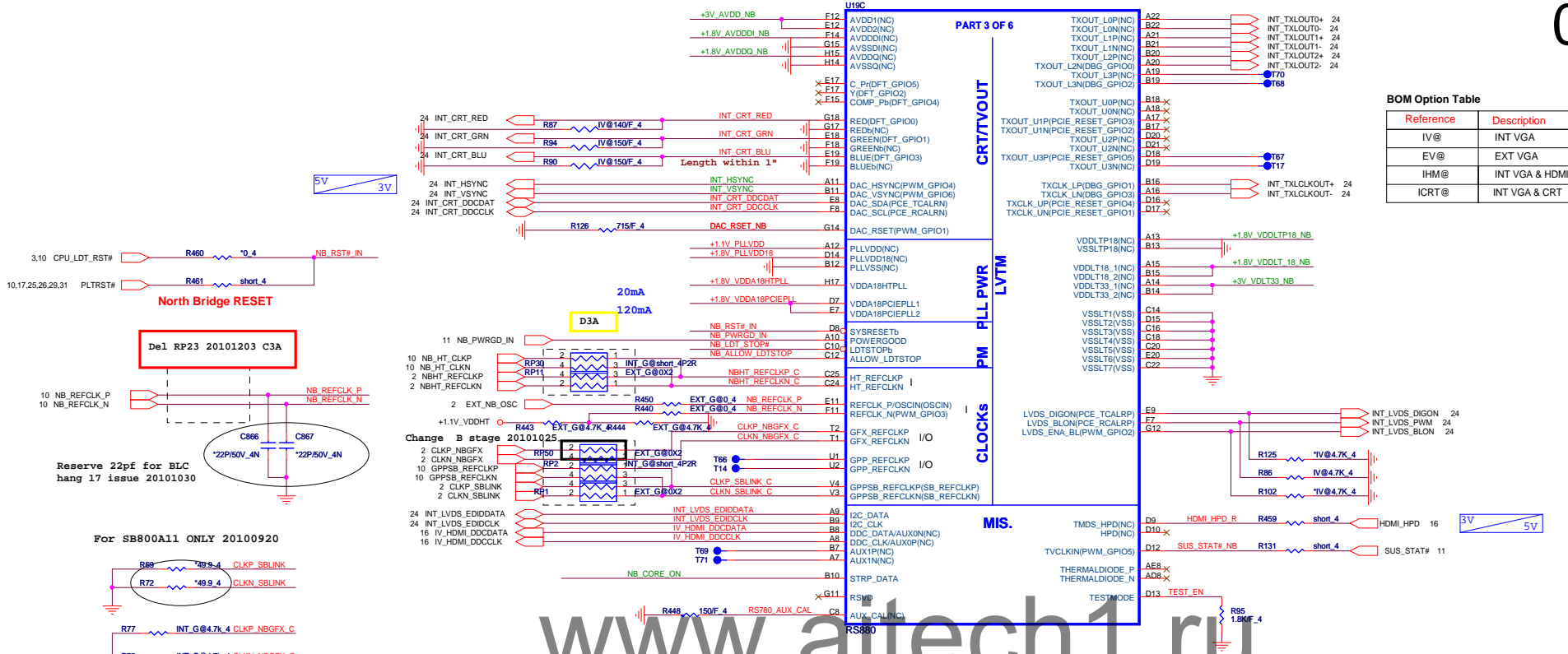
C PEG_TXP15	C234	IHM@0.1U/10V_4X	INT_HDMITX2P	16
C PEG_TXN15	C229	IHM@0.1U/10V_4X	INT_HDMITX2N	16
C PEG_TXP14	C232	IHM@0.1U/10V_4X	INT_HDMITX1P	16
C PEG_TXN14	C233	IHM@0.1U/10V_4X	INT_HDMITX1N	16
C PEG_TXP13	C236	IHM@0.1U/10V_4X	INT_HDMITX0P	16
C PEG_TXN13	C237	IHM@0.1U/10V_4X	INT_HDMITX0N	16
C PEG_TXP12	C230	IHM@0.1U/10V_4X	INT_HDMICLK+	16
C PEG_TXN12	C231	IHM@0.1U/10V_4X	INT_HDMICLK-	16

To HDMI CONN

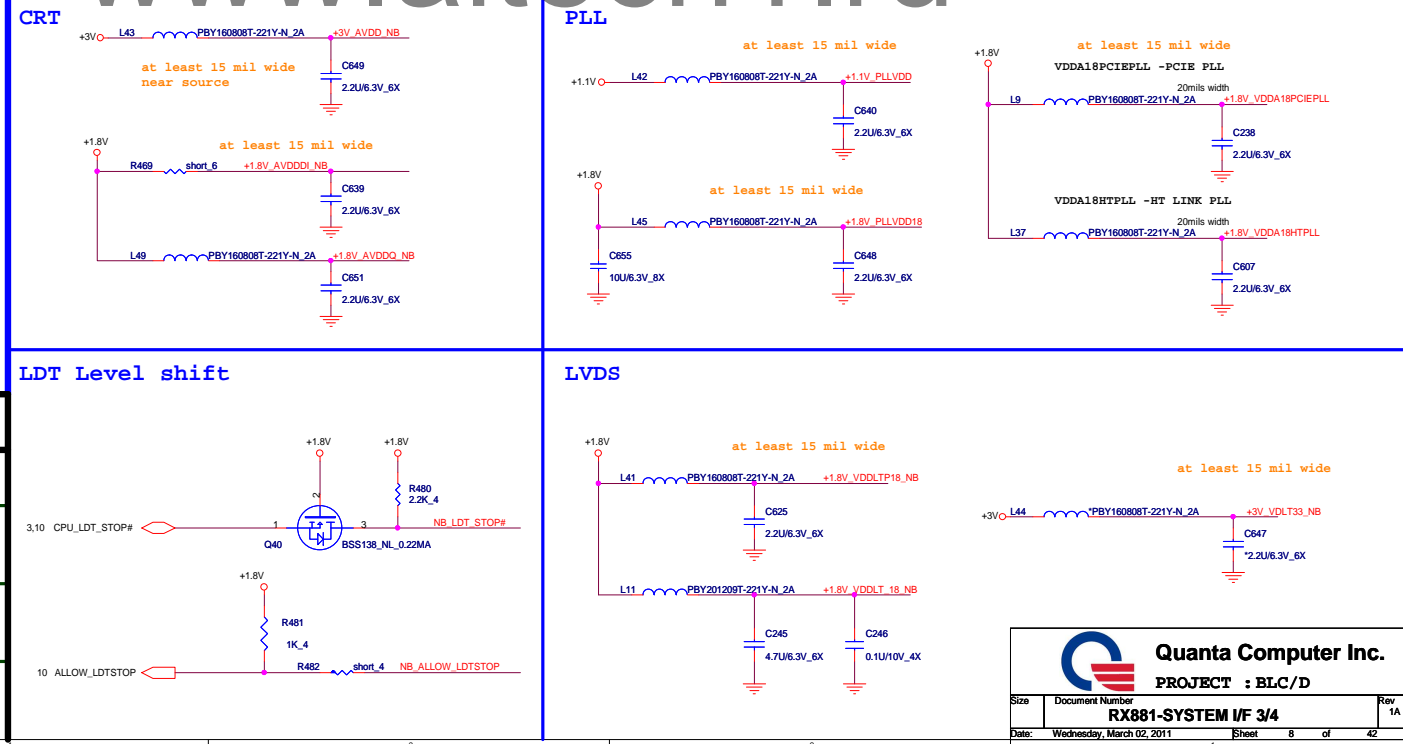


Quanta Computer Inc.

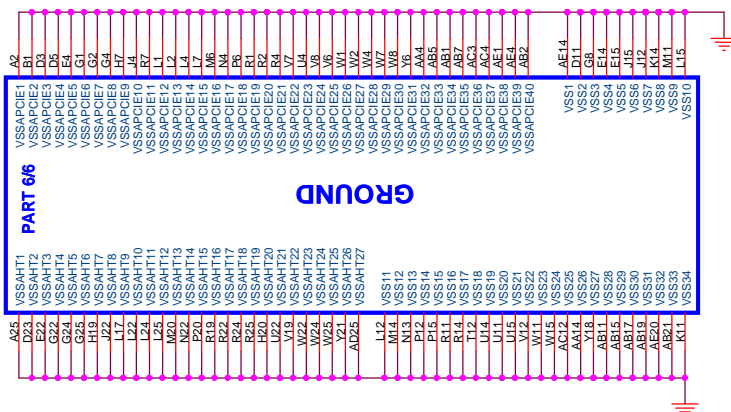
PROJECT : BLC/D



www.aitech1.ru

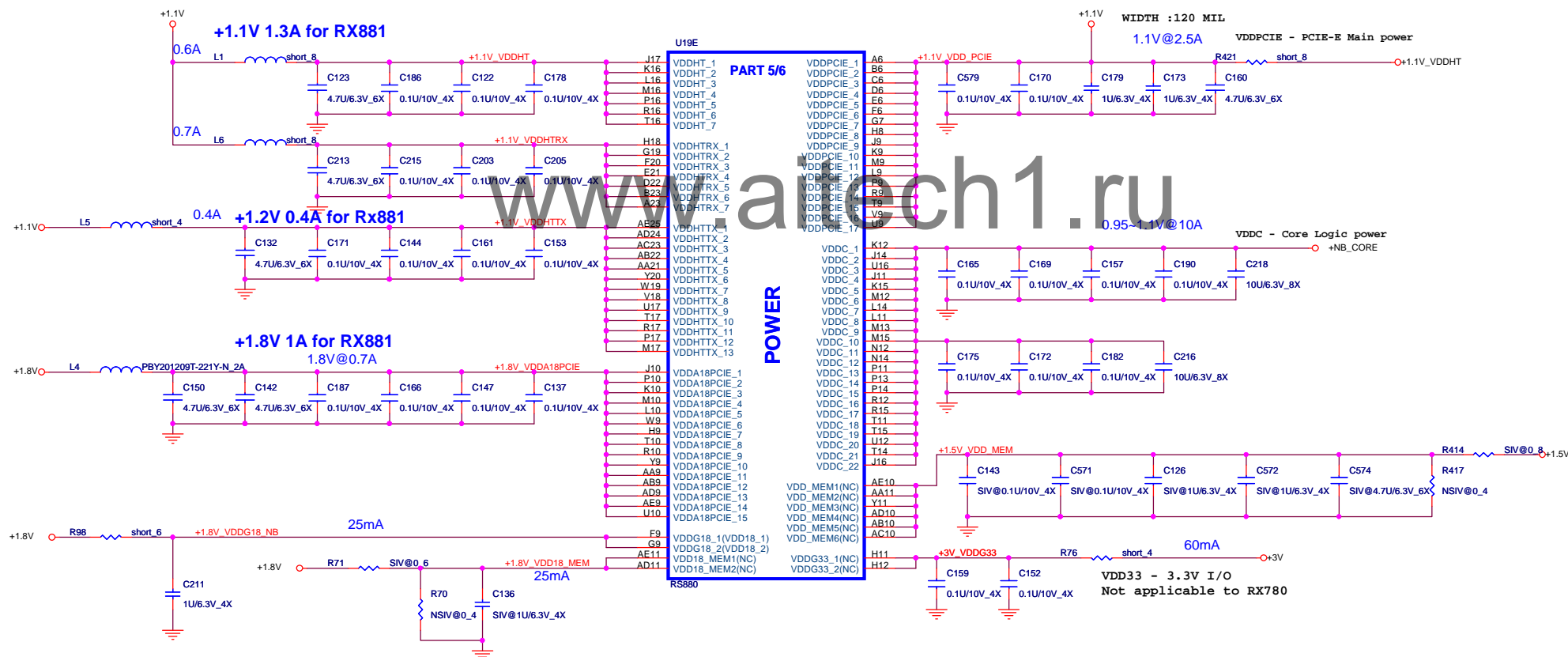


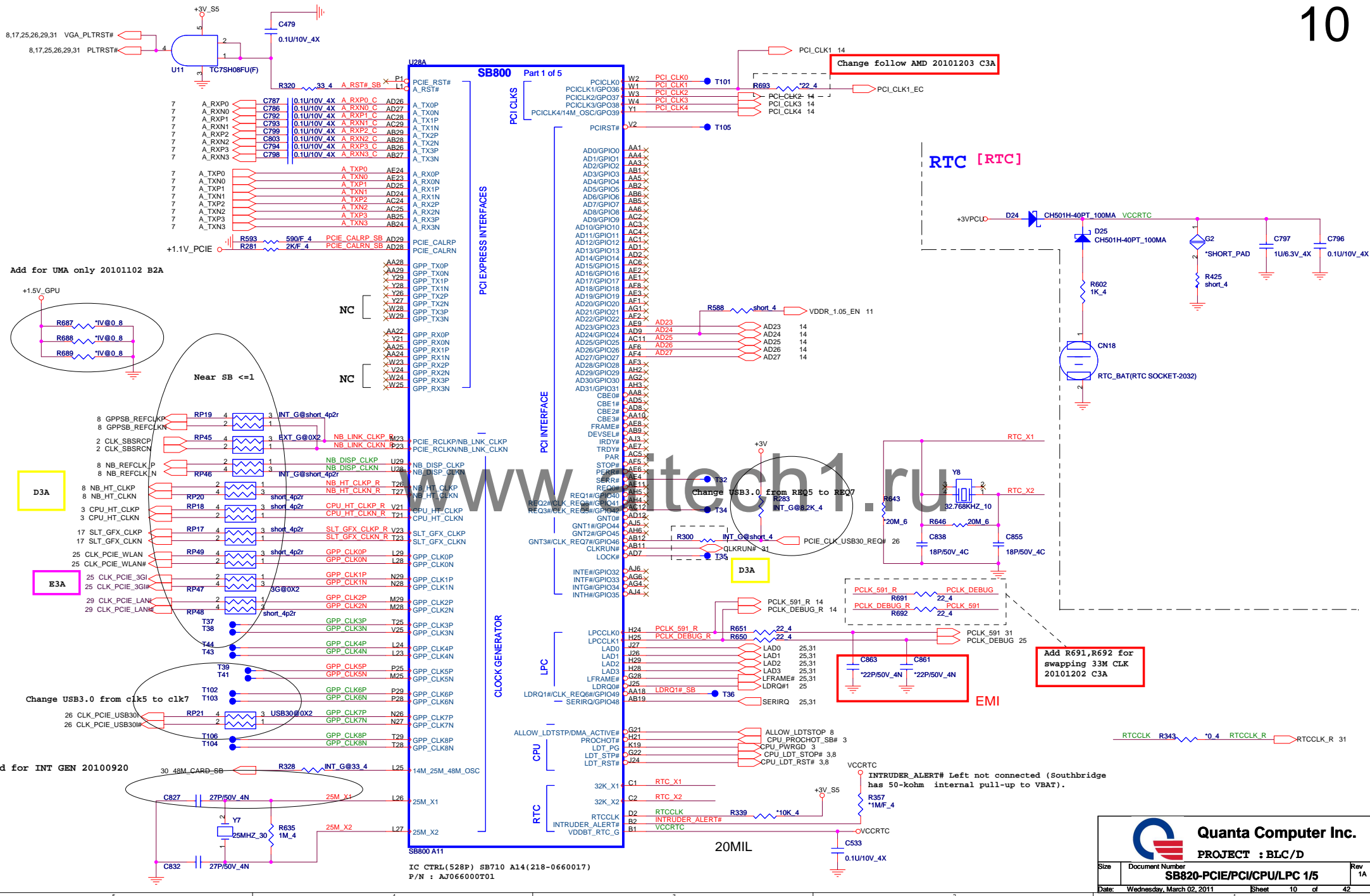
U19F



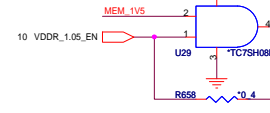
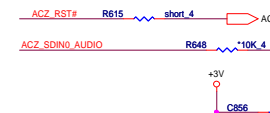
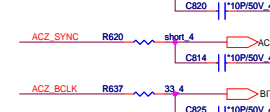
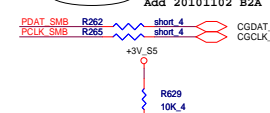
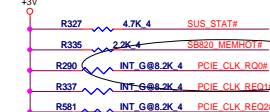
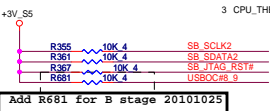
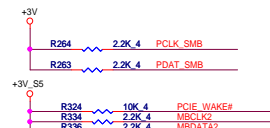
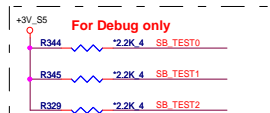
### RS880 POWER DIFFERENCE TABLE

PIN NAME	RS880	PIN NAME	RS880
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	1.5V	VDDLT18	+1.8V
VDDG33	+3.3V	VDDLTP18	+1.8V
IOPLLVD18	+1.8V	VDDLTP33	NC

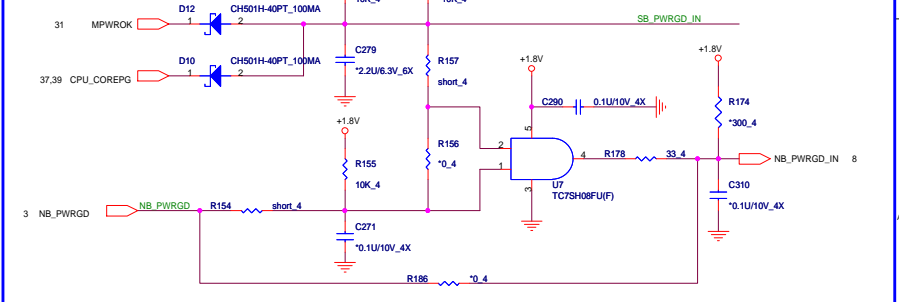
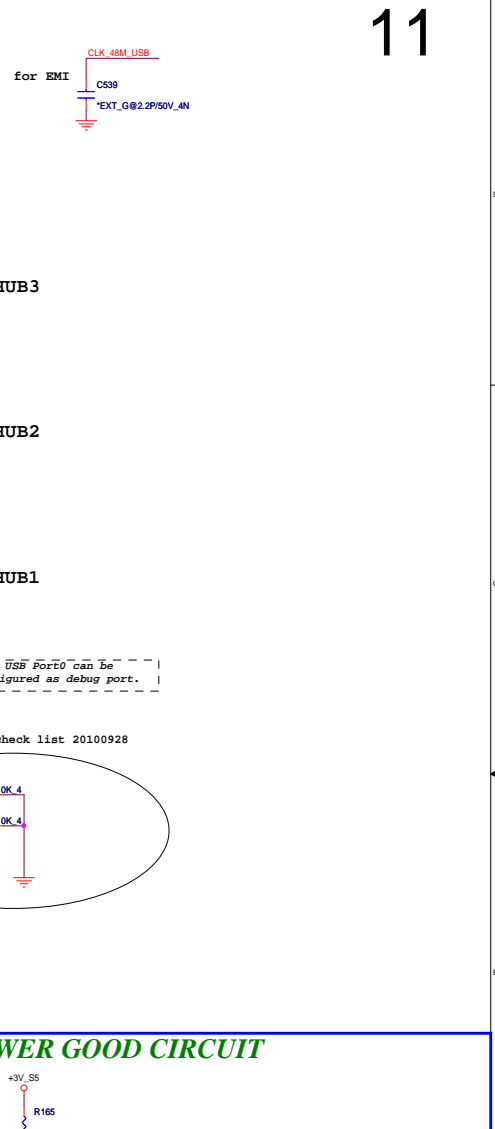
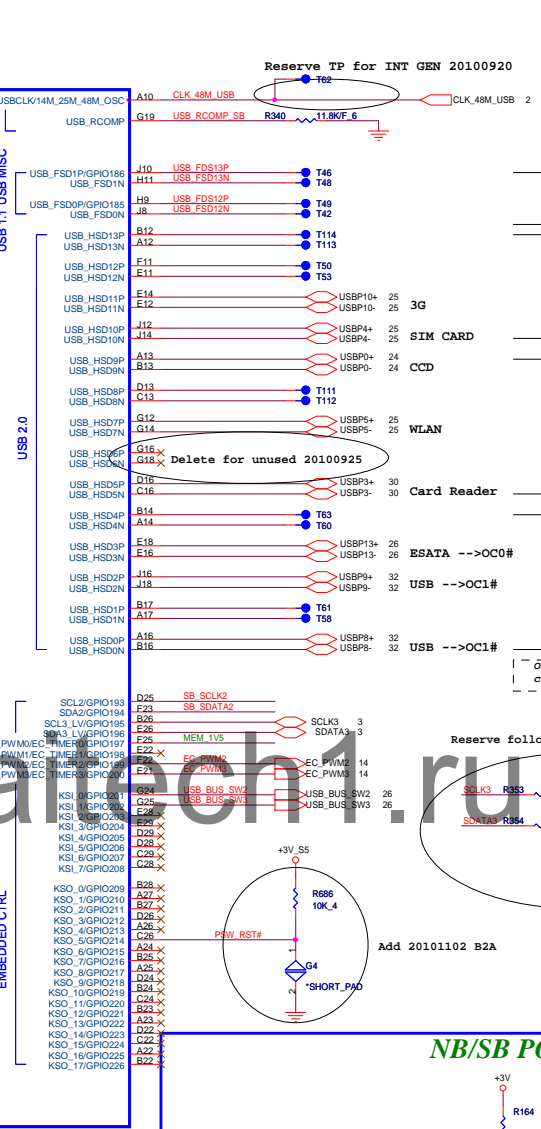
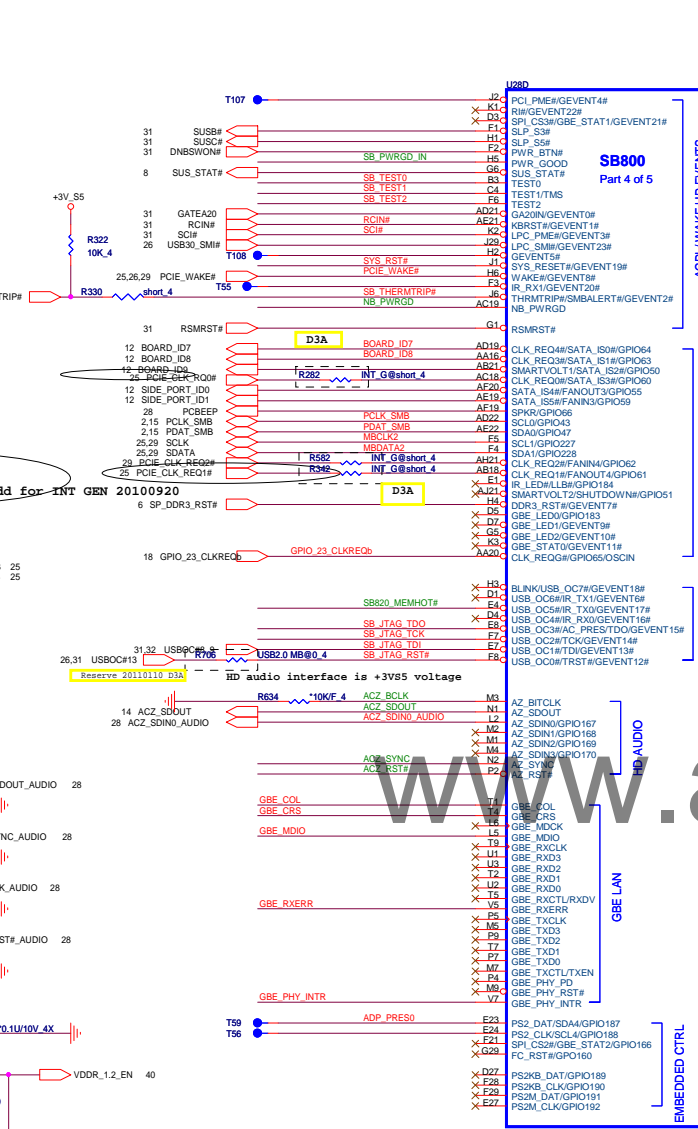








SMBUS	Assign Component
SMBUS0	CLK Gen. / DDR3 / WiFi
SMBUS1	LAN
SMBUS2	
SMBUS3	Sideband TSI



SATA PORT 0,1,2,3 can support AHCI mode

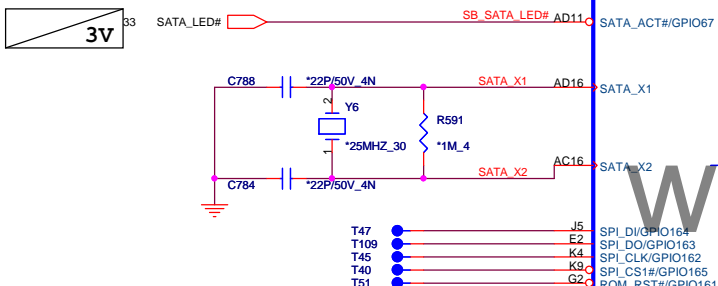
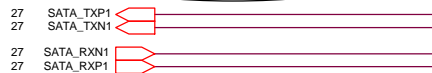
## SATA HDD



## E-SATA

Delete SATA2 for on E-SATA 20100919

## SATA ODD



U288

## SB800

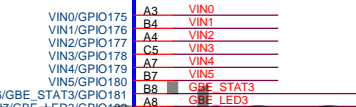
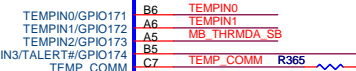
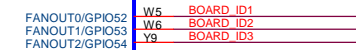
Part 2 of 5

SERIAL ATA

HW MONITOR

SPI ROM

SB800 A11



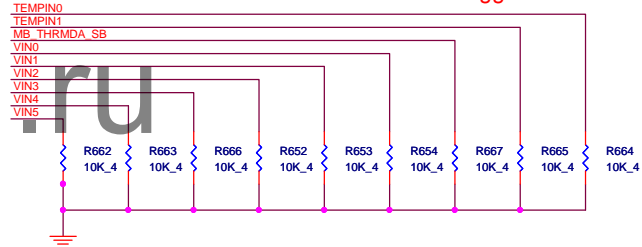
PLACE SATA\_CAL  
RES VERY CLOSE  
TO BALL OF SB820

12

IF THERE IS NO IDE, TEST  
POINTS FOR DEBUG BUS  
IS MANDATORY



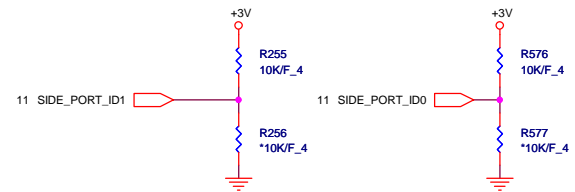
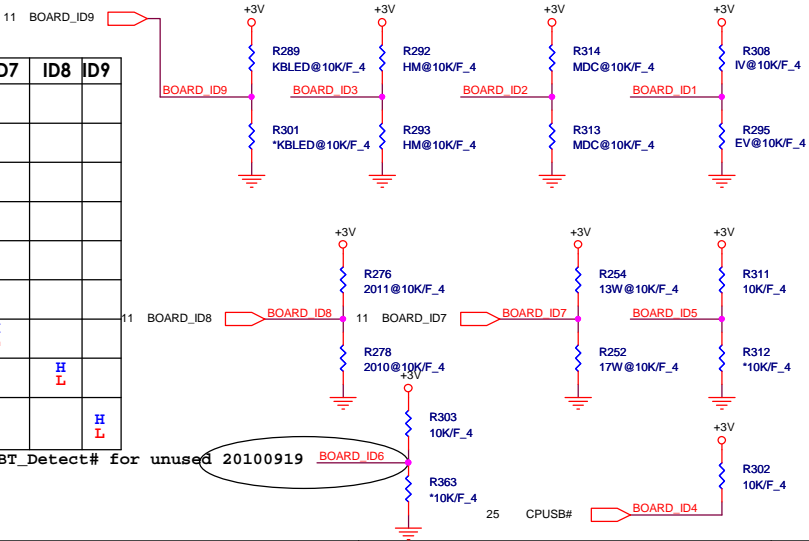
Follow AMD suggestion



## BOARD ID SETTING

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
UMA SKU VGA SKU	H	L							
W/ MDC W/O MDC		H	L						
W/ HDMI W/O HDMI			H	L					
W/O 3G W/ 3G				H	L				
15" 14"					H	L			
W/O BT W/ BT						H	L		
13W 17W							H	L	
2011 2010								H	L
W/O KBLED W/ KBLED									H

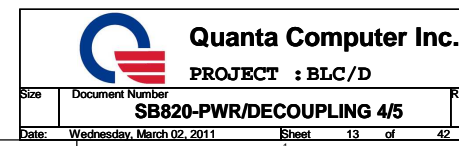
Delete BT\_Detect# for unused 20100919 BOARD\_ID6



ID1	ID0	Function
0	0	Samsung
0	1	Hynix
1	0	Reserve
1	1	No sideport support



Quanta Computer Inc.  
PROJECT : BLC/D



## REQUIRED STRAPS



OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.

14

Ball Name	Strap Name	Default	Description	Setting
LPCCLK0	ECEnableStrap	0	0 -- Disable 1 -- Enable Enable to support enhanced hardware monitor feature	10 PCLK_591_R +3V_S50 R668 *10K/F 4 R671 10K/F 4
EC_PWM3 EC_PWM2	ROMTYPE_1 ROMTYPE_0	(0,1)	(0,0) = Firmware Hub (0,1) = LPC (1,0) = SPI (1,1) = Reserved	11 EC_PWM3 +3V_S50 R358 *10K/F 4 R356 2.2K 4 11 EC_PWM2 +3V_S50 R341 *10K/F 4 R338 2.2K 4
LPCCLK1	CLKGEN	0	0 -- External clock 1 -- Integrate clock	10 PCLK_DEBUG_R +3V_S50 R649 INT_G@10K/F R655 EXT_G@10K/F 4
PCICLK1	BIF_GEN2_COM PLIANCE_Strap	1	0 -- PCIE at Gen I mode 1 -- PCIE at Gen II mode	10 PCI_CLK1 +3V_S50 R611 *10K/F 4 R612 10K/F 4
PCICLK2	BootFailTmeEn	0	0 -- Disable watchdog function 1 -- Enable watchdog function	10 PCI_CLK2 +3V_S50 R609 *10K/F 4 R607 10K/F 4
PCICLK3	DefaultStrapMode	0	0 -- Disable debug Straps 1 -- Select ext. Debug Straps	10 PCI_CLK3 +3V_S50 R600 *10K/F 4 R604 10K/F 4
PCICLK4	CPUClkSel	1	0 -- Reserved 1 -- Integrated clock mode	10 PCI_CLK4 +3V_S50 R605 *10K/F 4 R601 10K/F 4
AZ_SDOUT	CoreSpeedMode	0	0 -- Performance mode 1 -- Low Power mode	11 ACZ_SDOUT +3V_S50 R626 *10K/F 4 R623 10K/F 4

SB820M only support Gen I

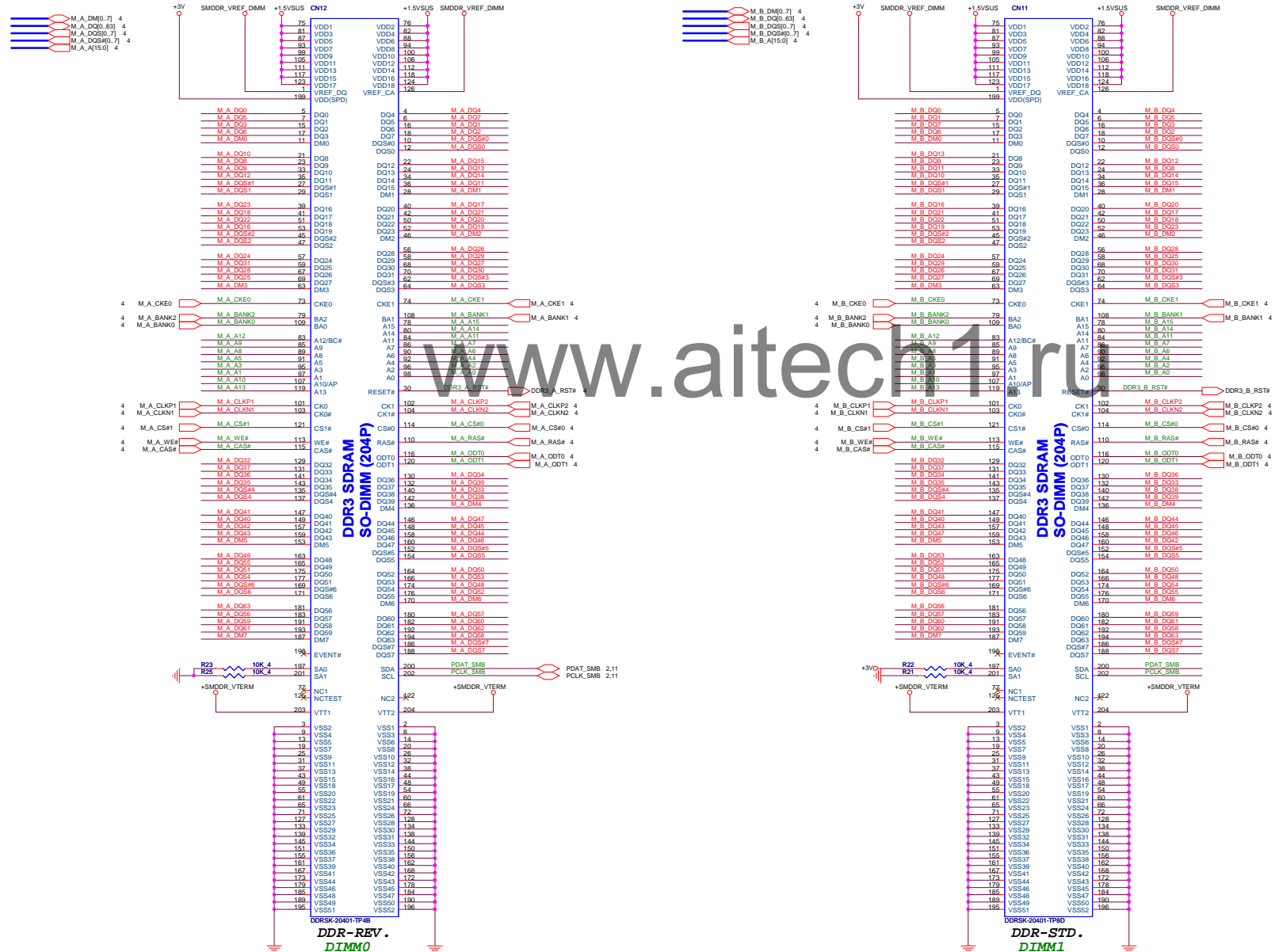
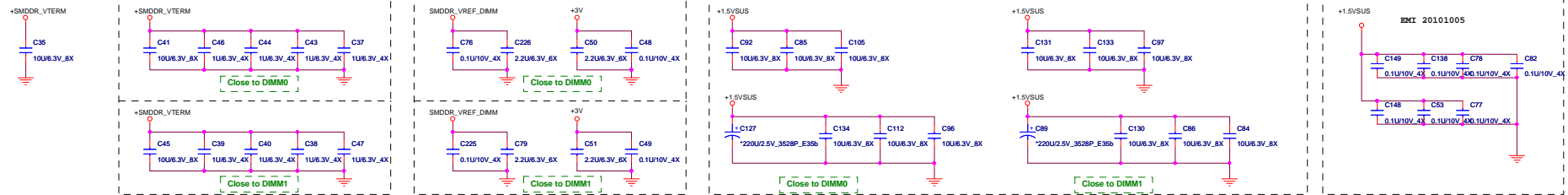
## DEBUG STRAPS

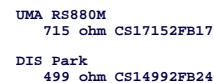
SB800 HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

Ball Name	Strap Name	Default	Description	Setting
AD27	PciPl1Byp	1	0 -- ByPass Int PLL 1 -- Int. PLL	10 AD27 +3V_S50 R599 10K/F 4 R596 1 2.2K 4
AD26	ILAAutronEnB	1	0 - IAL auto run enable 1 -- IAL auto run disable	10 AD26 +3V_S50 R590 10K/F 4 R589 1 2.2K 4
AD25	FCClkByP	1	0 -- Bypass FC Clk 1 -- Int. FC Clk	10 AD25 +3V_S50 R592 10K/F 4 R595 1 2.2K 4
AD24	I2CRomEn	1	0 -- Enable EEPROM 1 -- Disable EEPROM	10 AD24 +3V_S50 R586 10K/F 4 R587 1 2.2K 4
AD23	PCI_ROM_BOOT	1	0 -- Disable PCI MEM Boot 1 -- Enable PCI MEM Boot	10 AD23 +3V_S50 R585 10K/F 4 R584 1 2.2K 4
All signals ihas nternal PU				

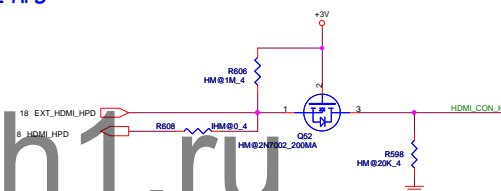
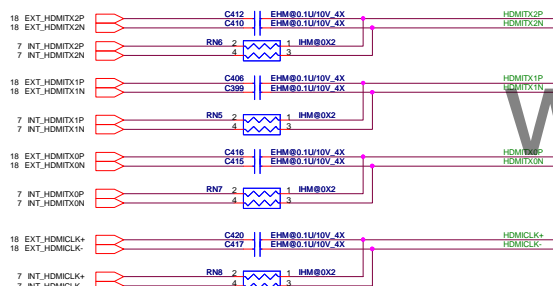


Quanta Computer Inc.  
PROJECT : BLC/D

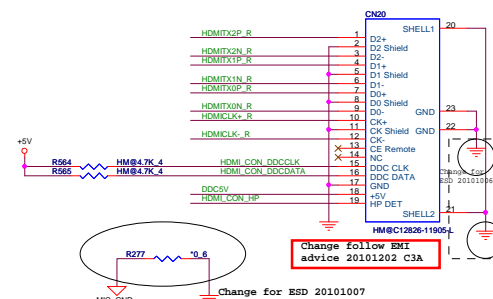
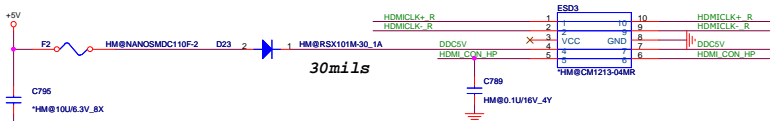
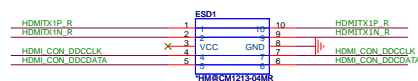
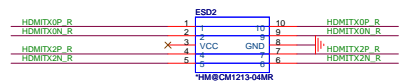
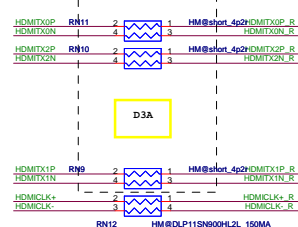
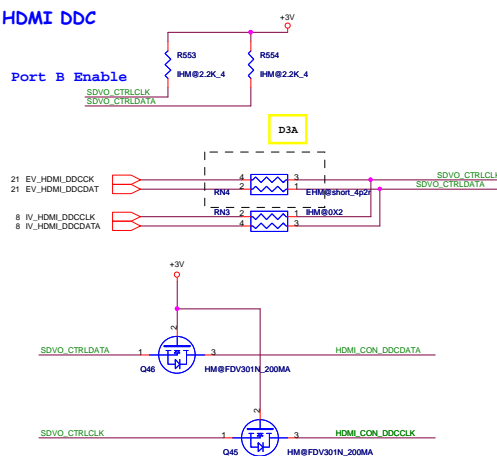




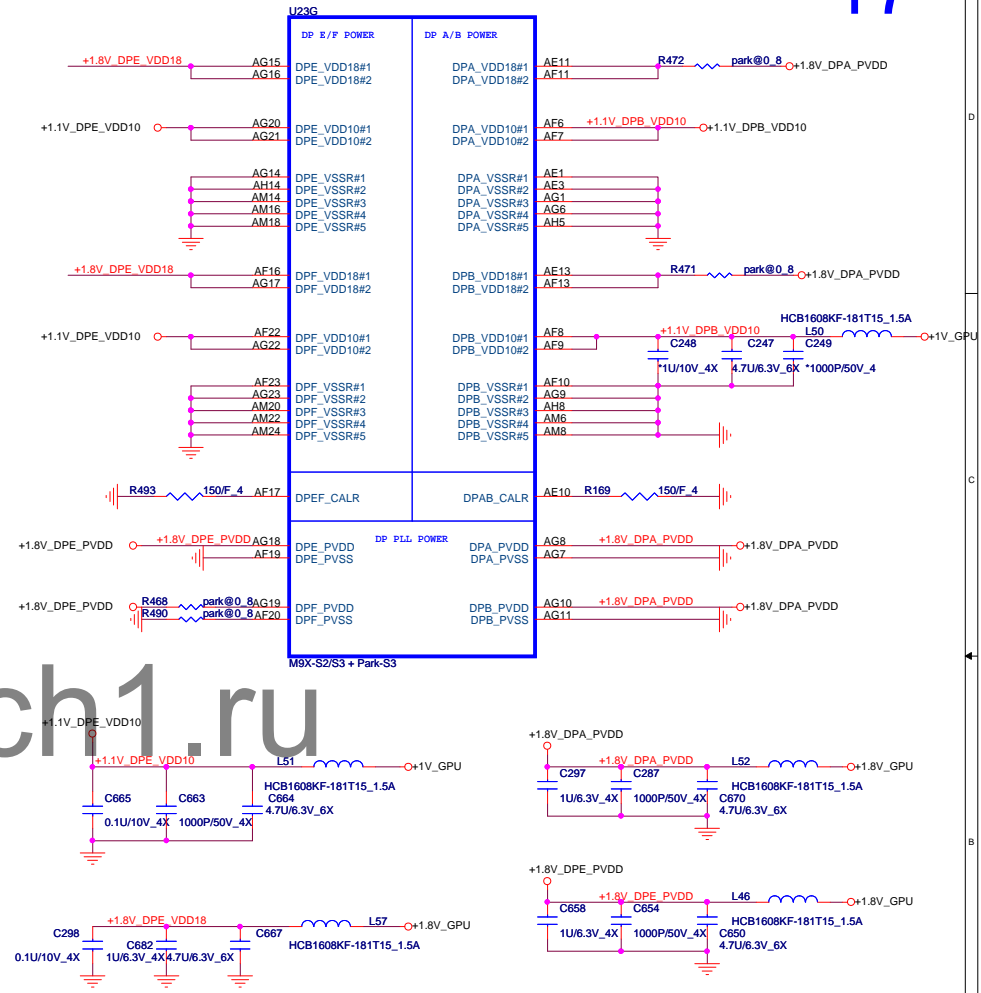
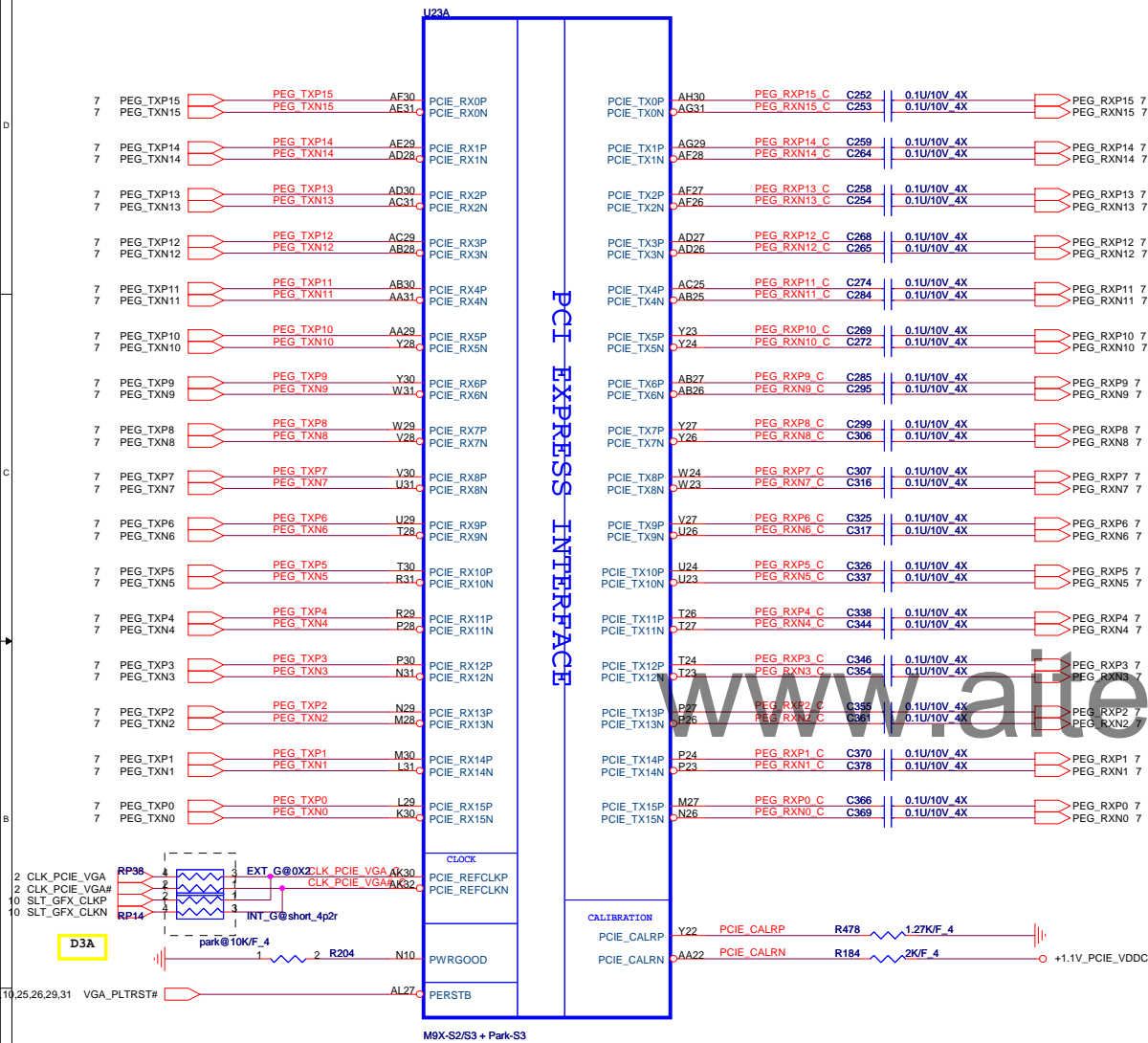
## HDMI HPD



Close to HDMI CONN



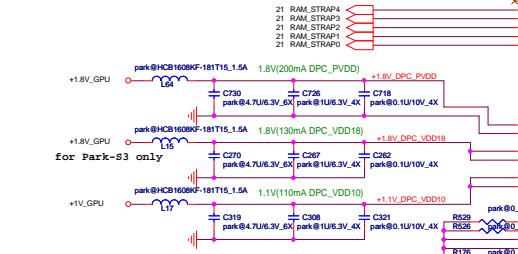




Quanta Computer Inc.

PROJECT : BLC/D

Size	Document Number	Rev
	M93-S3_PCIE_Interface	1A
Date	Wednesday, March 02, 2011	Sheet 17 of 42



GPIO13 R544 \*10K/F\_4

GPIO12 R541 \*10K/F\_4

GPIO11 R542 \*10K/F\_4

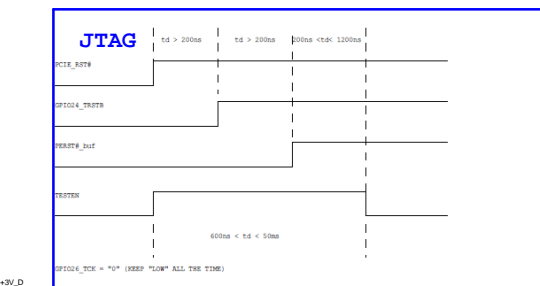
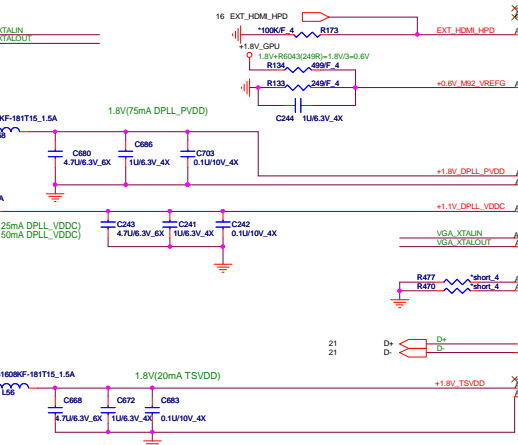
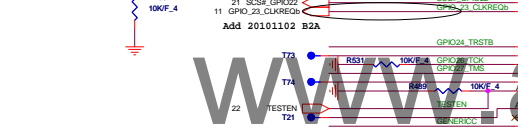
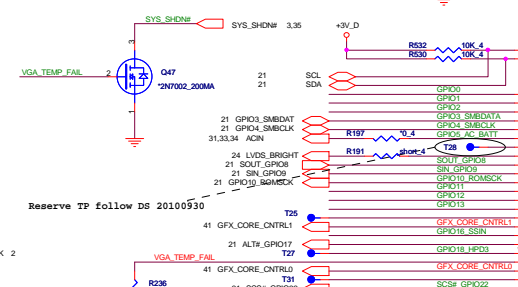
TESTEN R227 \*10K/4


GPIO27 TMS R552 \*10K/4

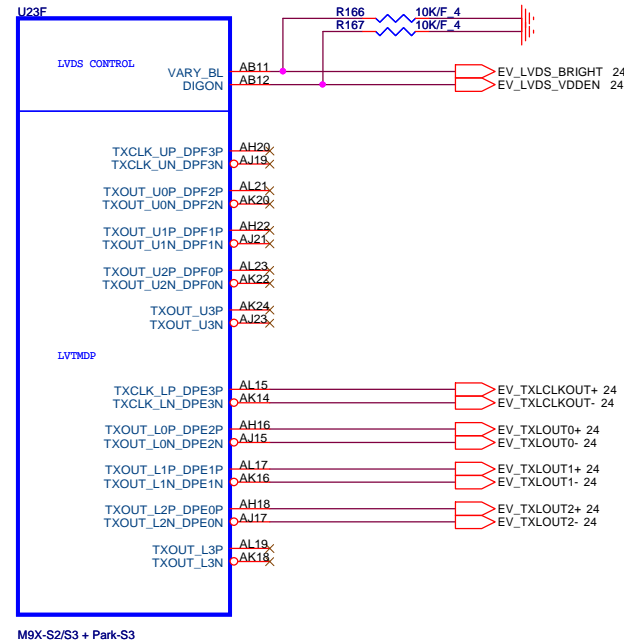
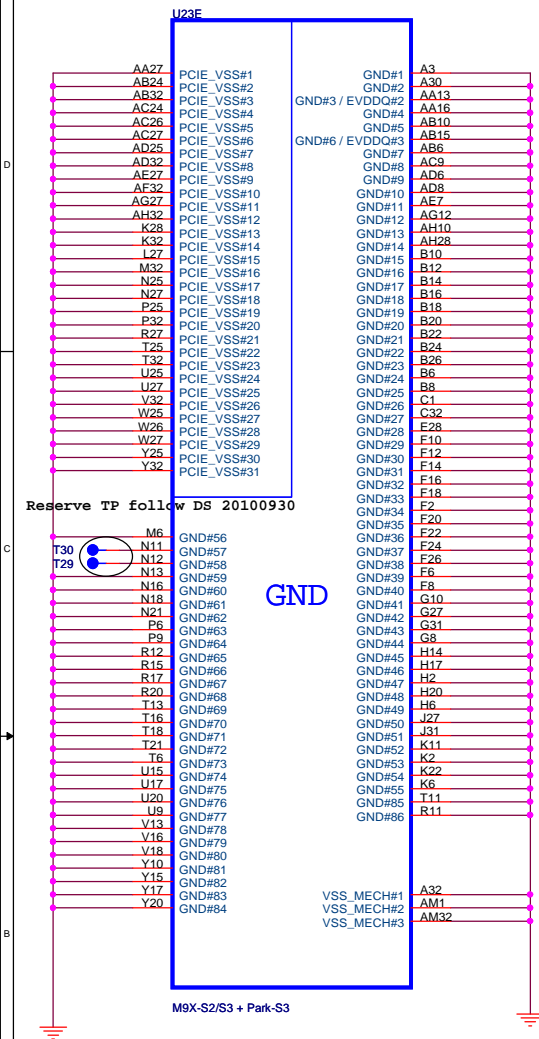
R535 \*10K/4

GPIO26 TCK R540 \*0.4

GPIO24 TRSTB R555 \*10K/4




**Quanta Computer Inc.**  
**PROJECT : BLC/D**  
 Size: Document Number: M93-S3\_Main  
 Date: Wednesday, March 02 2011 Sheet: 18 of 42



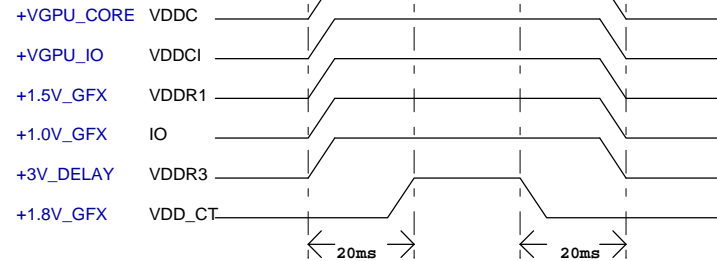
Strap Name	Pin	Straps description	Default Value
TX_PWRS_ENB	GPIO0	<b>PCI Express Full TX Output Swing</b> 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	<b>PCI Express Transmitter De-emphasis Enable</b> 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	1
RSVD	GPIO8	<b>Enable CLKREQ# Power Management</b> 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
BIF_VGA_DIS	GPIO9		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	1
AUD[0] AUD(1)	VSYN HSYN	<b>AUD[1] AUD[0]</b> 00 No Audio function 01 Audio for DisplayPort and HDMI if dongle is detected 10 Audio for DisplayPort only 11 Audio for both DisplayPort and HDMI	1 1
VIP_DEVICE_STRAP_ENA	V2SYN	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0
RSVD	GENERIC		0

www.aitech1.ru

Power Up/Down Sequence

### GPU Power-on sequence

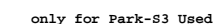
- 1 => +3V\_DELAY
- 2 => +VGPU\_CORE
- 3 => +VGPU\_IO
- 4 => +1V\_GPU
- 5 => +1.5V\_GPU
- 6 => +1.8V\_GPU
- 7 => dGPU\_PWROK



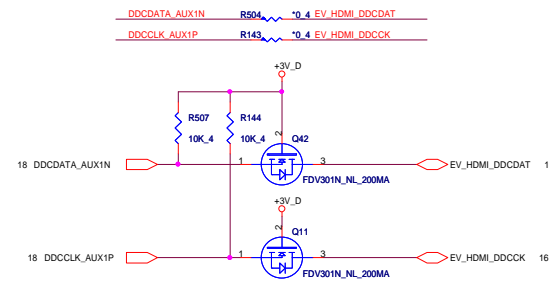
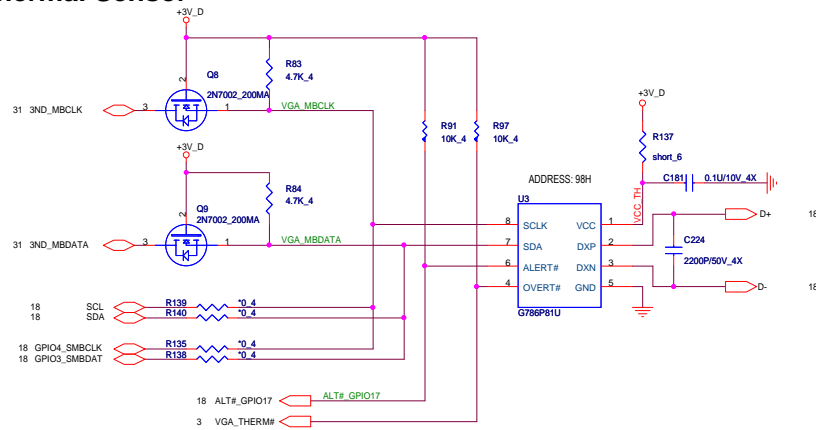
Quanta Computer Inc.

PROJECT : BLC/D

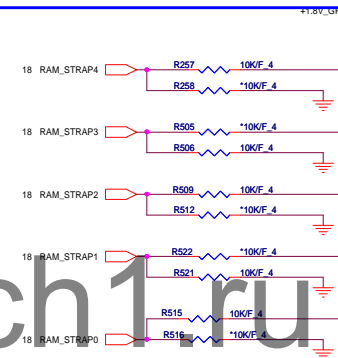
Size	Document Number	Rev
	M93-S3_GND / LVDS/ Straps	1A
Date:	Wednesday, March 02, 2011	Sheet 19 of 42



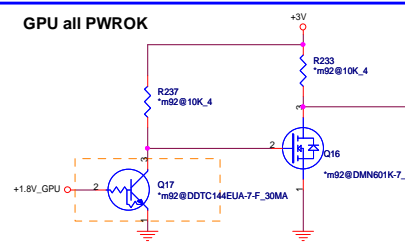
## VRAM Memory TYPE



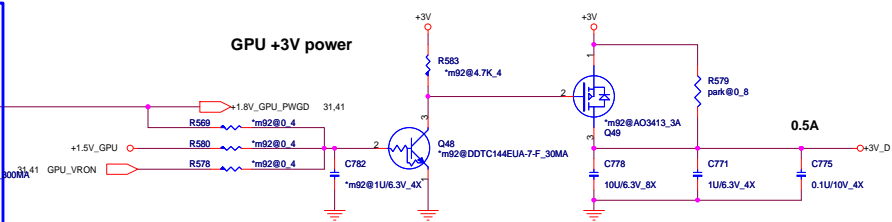
Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3	RAM_STRAP2	RAM_STRAP1	RAM_STRAP0	RAM_STRAP4	
				DVPDATA_3	DVPDATA_2	DVPDATA_1	DVPDATA_0	15"	14"
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW00 (64M*16)	512MB	0	1	0	0	0	1
			1GB	0	0	0	0	0	1
		AKD5MGGTW00	2GB	0	0	1	0	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT502 (64M*16)	512MB	0	1	0	1	0	1
			1GB	0	0	0	1	0	1
	K4W2G1646B-HC12	AKD5MGGT501	2GB	0	0	1	1	0	1



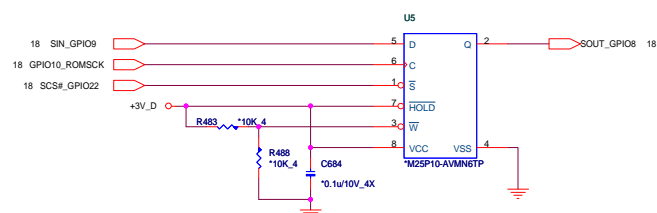
## GPU all PWROK

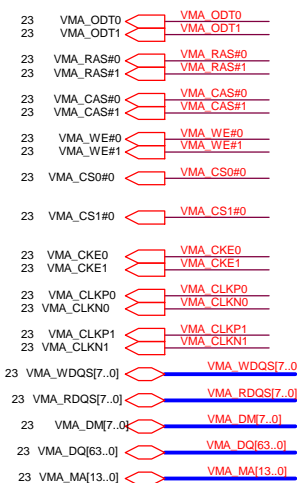


**GPU +3V power**

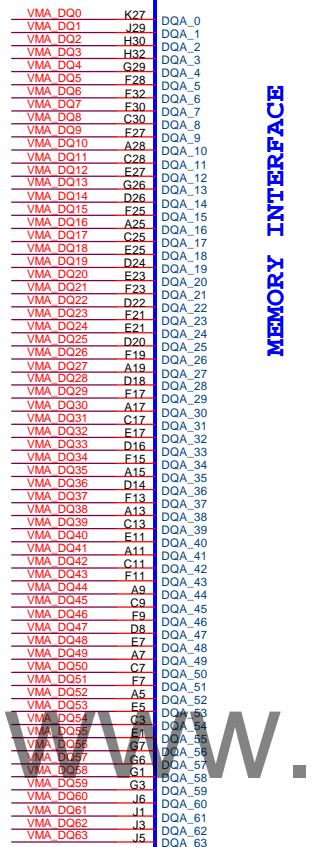


## EEPROM

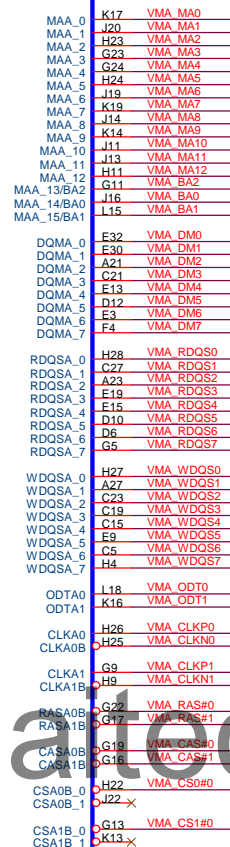




support 1Gbit  
VRAM ( 64M x 16 )



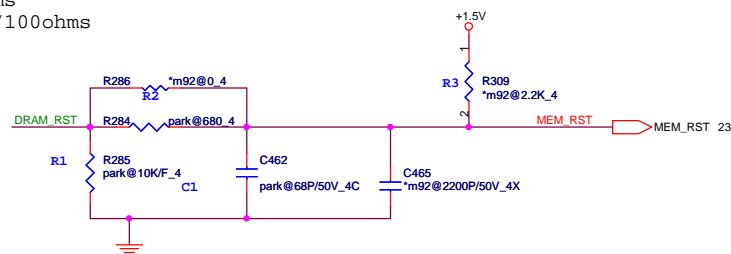
# MEMORY INTERFACE



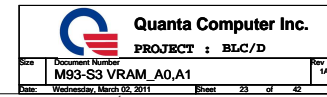
for Park-S3: Use only  
for M9x-S3: no support

for Park-S3: Use Cap  
0.1uF, Res 51.1R  
Routing 50ohms  
single-ended/100ohms  
diff

	M9x-S2/S3	Park-S3
MEM_CALRN0 (J25)	NC	240R
MEM_CALRP0 (K25)	NC	240R
MEM_CALRP1 (J8)	240R	150R
TESTEN2#2 (K7)	NC	0R
R1	NC	10K
R2	0R	680R
R3	2.2K	NC
C1	2.2nF	68pF

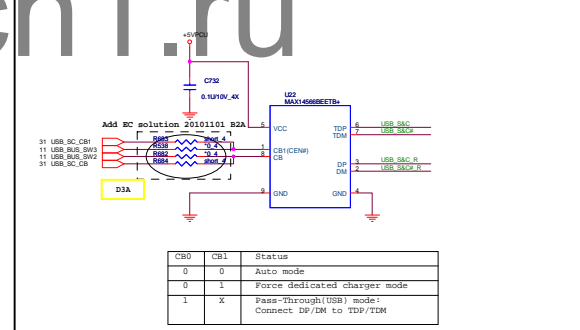








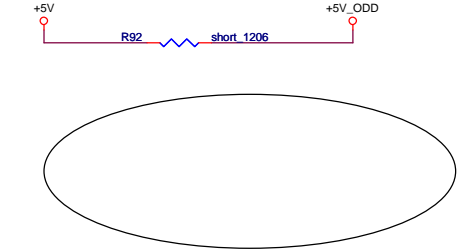
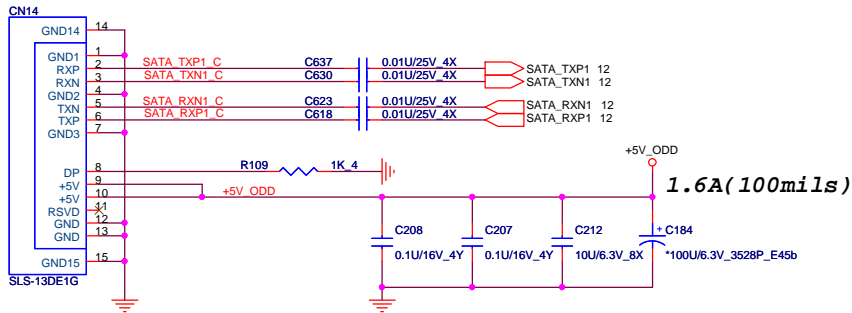




CB0	CB1	Status
0	0	Auto mode
0	1	Force dedicated charger mode
1	X	Pass-Through(USB) mode: Connect DP/DM to TDP/TDM

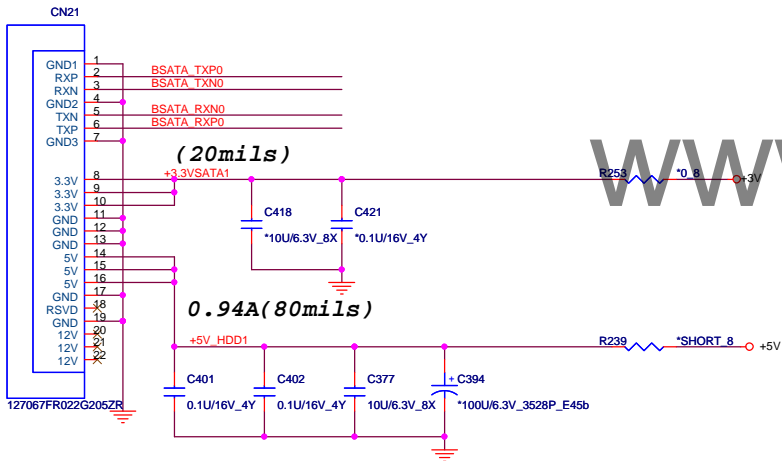
SATA ODD

ODD Zero power . (Only for Intel)<OZP>



Del the reserve circuit for ODD zero PWR 20101101 B2A

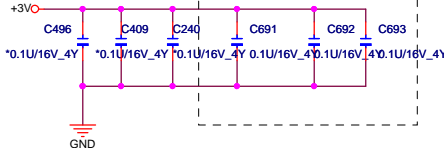
SATA HDD



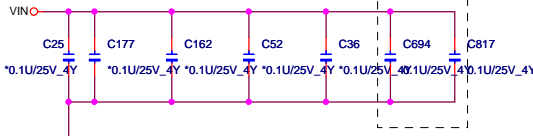
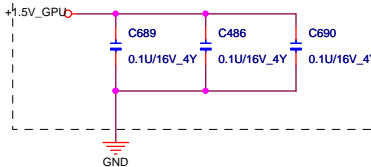
www.aitech1.ru

EMI

Add for EMI 20101207 C3A

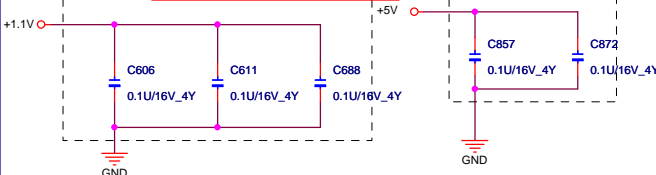


Add for EMI 20101207 C3A

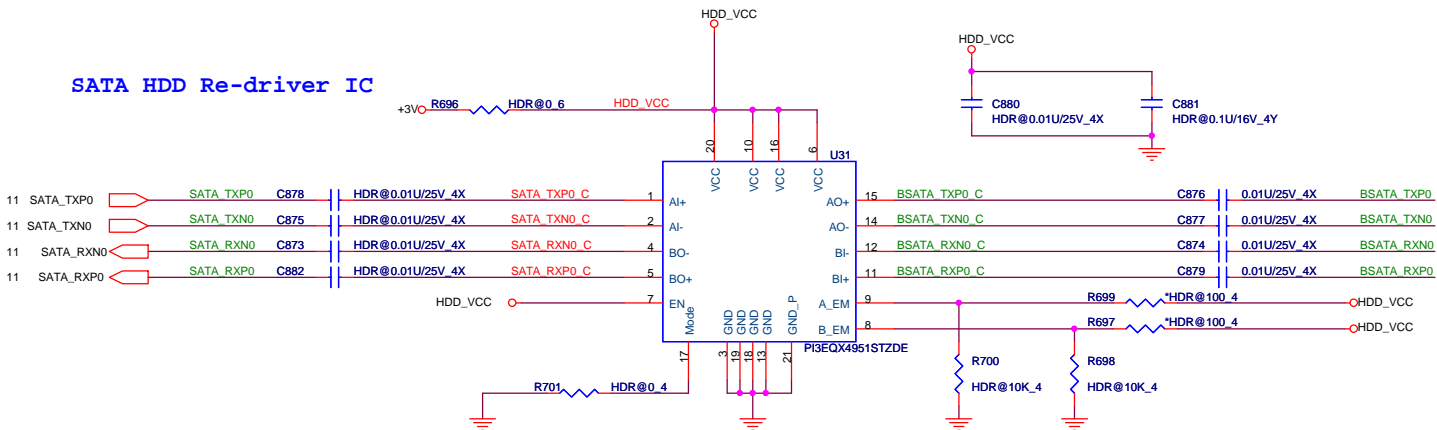


Add for EMI 20101207 C3A

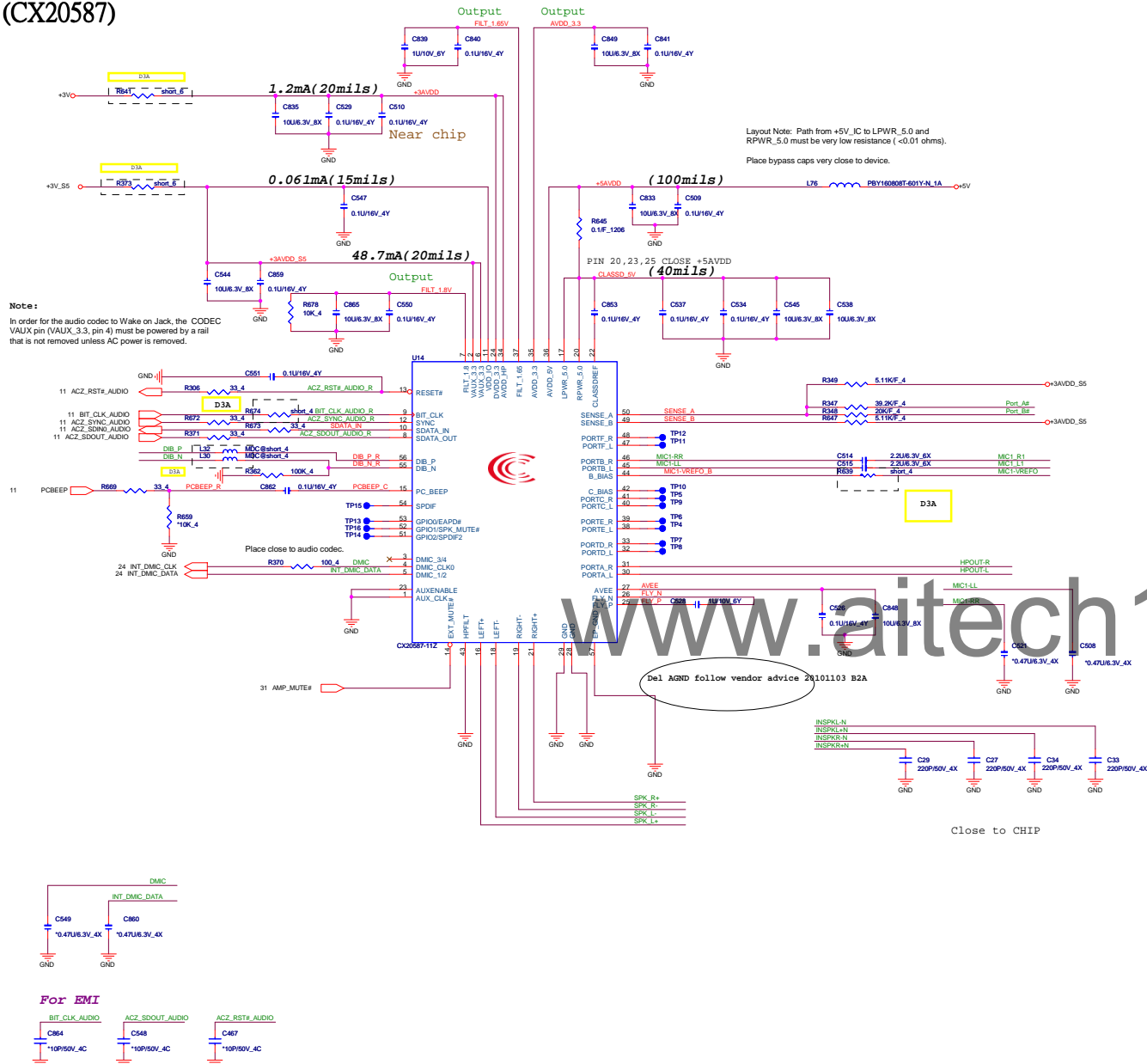
Add for EMI 20101207 C3A



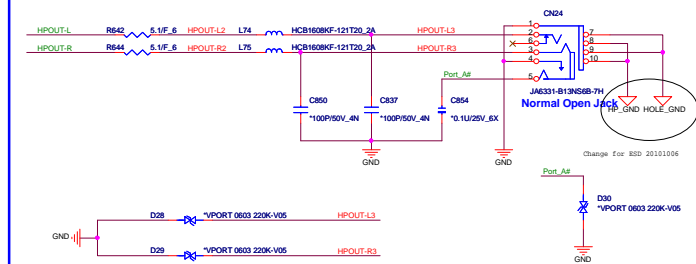
SATA HDD Re-driver IC



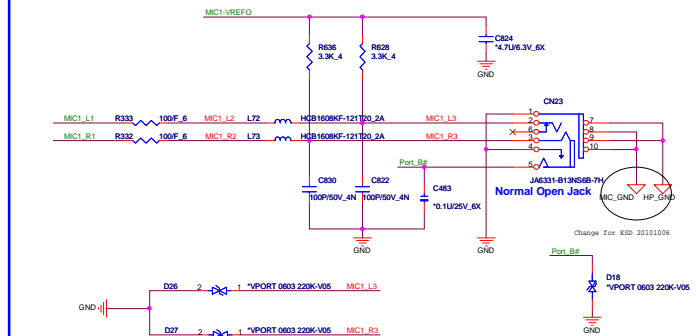
## AUDIO JACKS



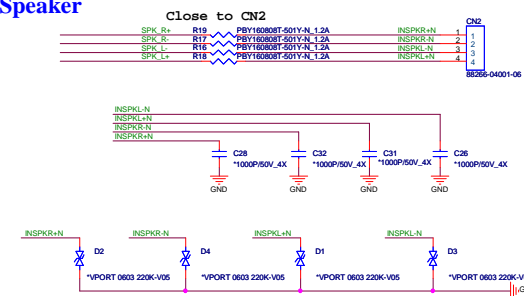
## Earphone



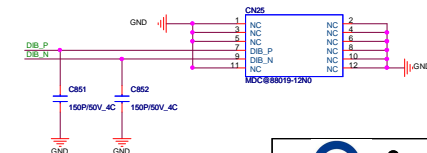
## External MIC



## Internal Speaker

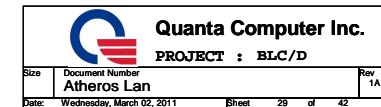


## MDC

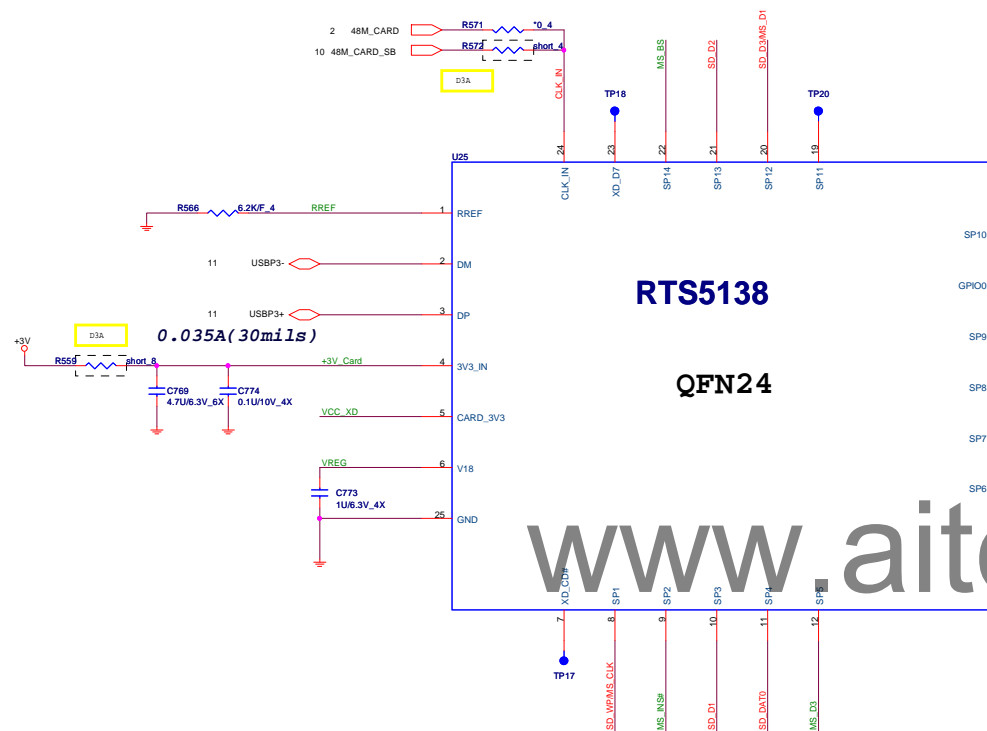




10/100 = 0 ohm CS00002JB38

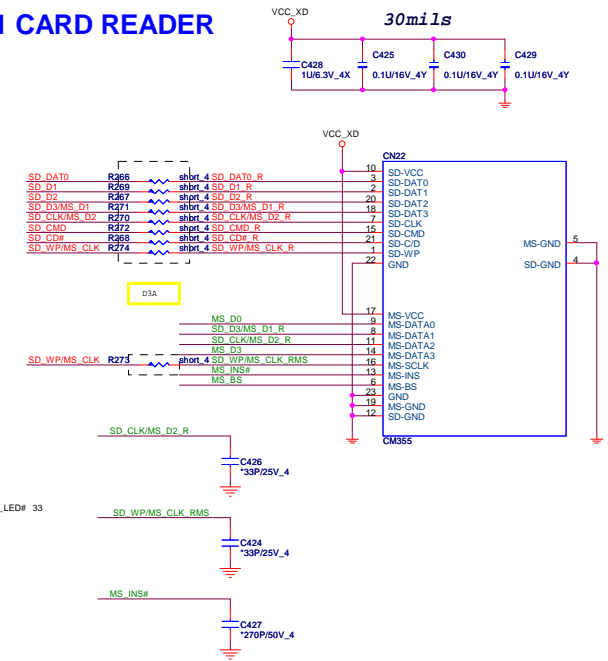


# 3 IN 1 CARD READER

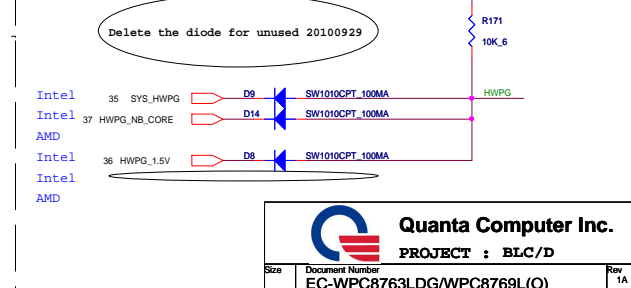
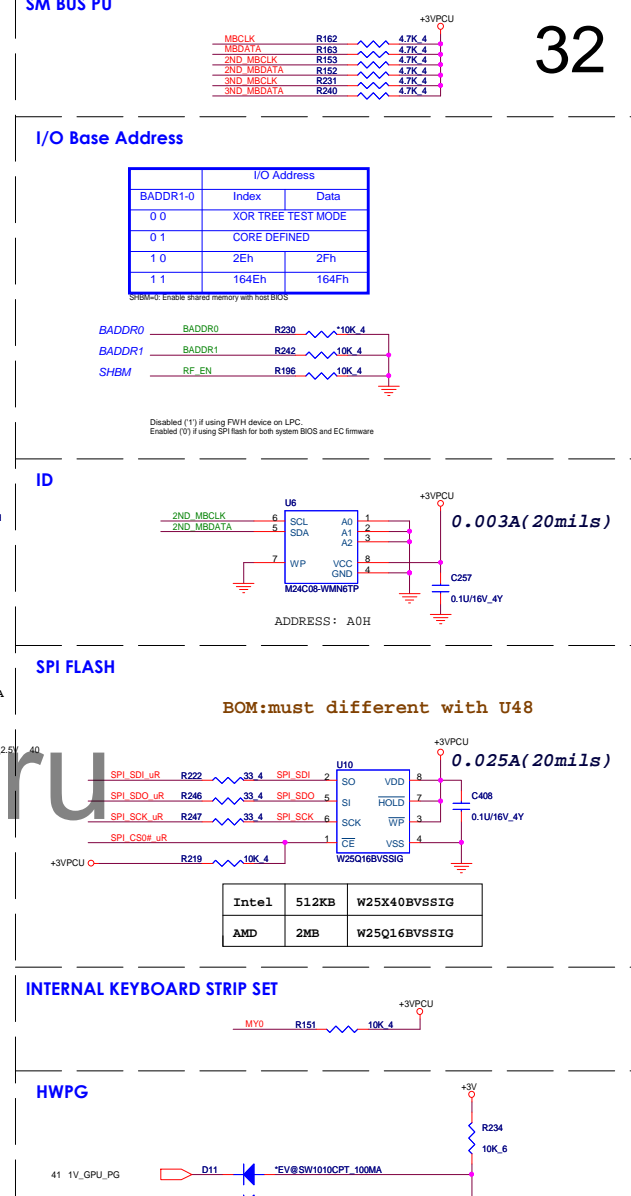


Add for cardreader  
LED behavior  
20101030

# 3 IN 1 CARD READER



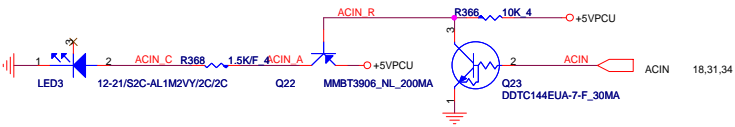
www.aitech1.ru



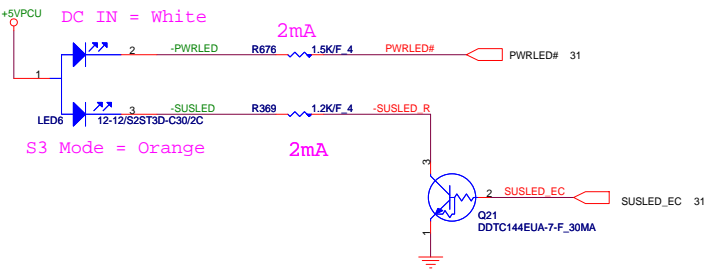


## LED

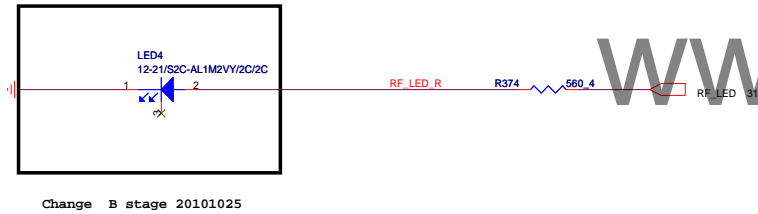
### AC-IN



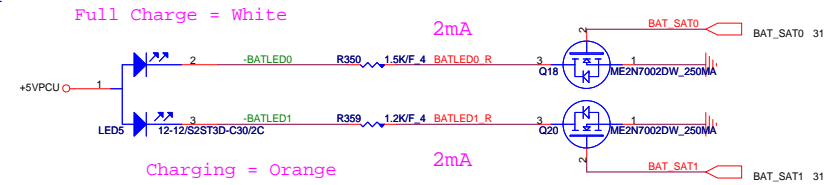
### POWER



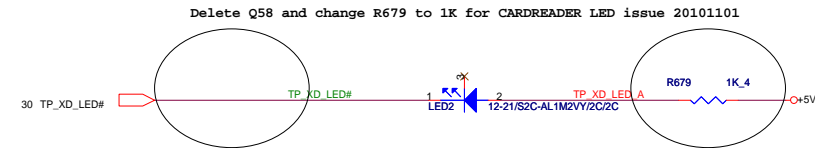
### RF LED



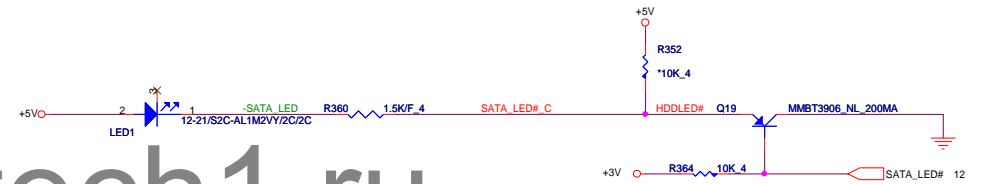
## BATTERY



## CARDREADER

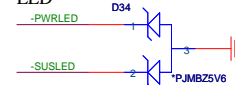


## HDD/ODD



### ESD Protect

#### FOR POWER LED



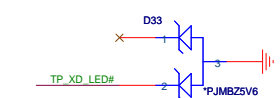
#### FOR BATTERY LED



#### FOR HDD/RF LED

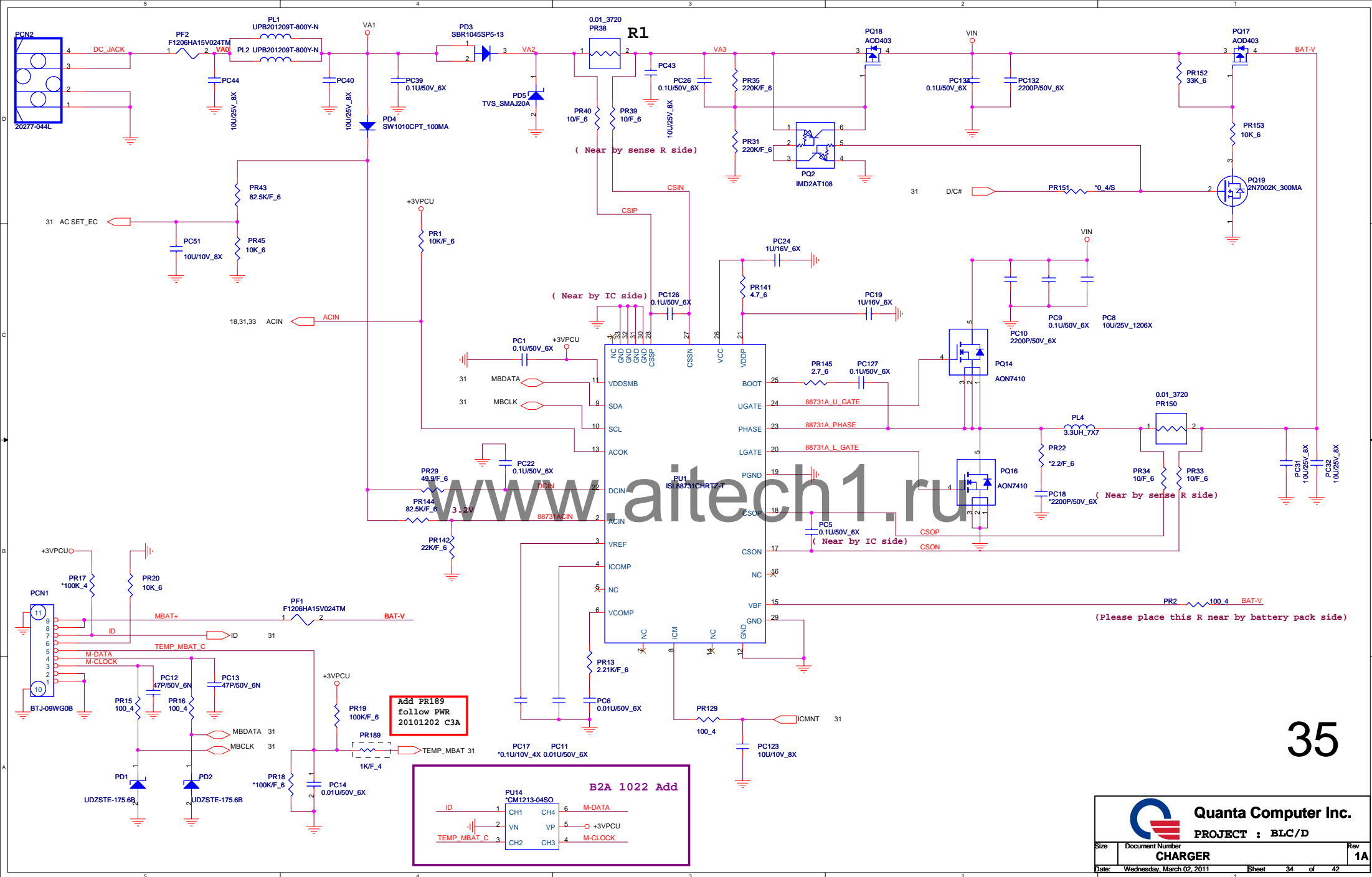


#### FOR CARDREADER LED



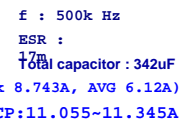
Quanta Computer Inc.

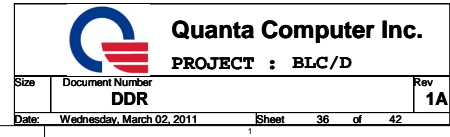
PROJECT : BLC/D

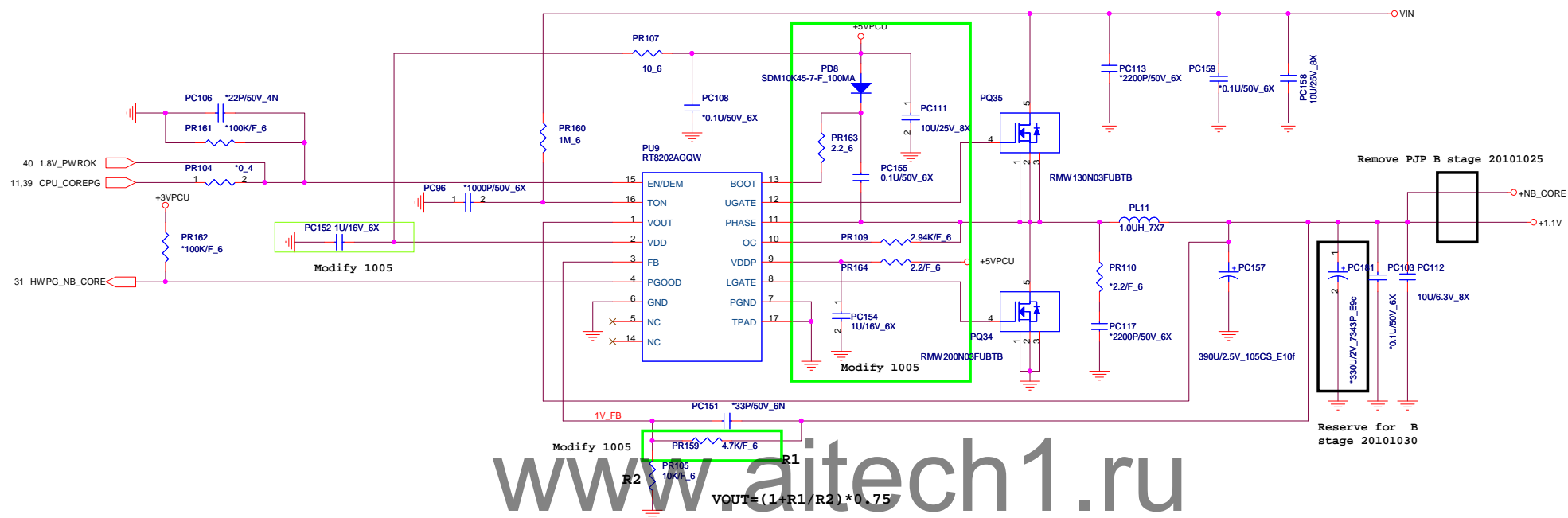


35









www.aitech1.ru

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	X	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

VDDNB Core (Peak 4A, AVG 2.8A) OCP 4.5A  
 OCP\_NB=ROCKET\*10uA/Rdson  
 ROCKET=PR34  
 OCP\_NB=11.3k\*10uA/23m=4.91A

ESR :  
 2m: 300k Hz  
 4A  
 +VDDNB\_CORE

3 CPU\_VDDNB\_FB\_H

3 CPU\_VDDNB\_FB\_L

+5VPCU

PR15 1U/25V\_8X

PR133 0.8/S

PR9 10/F\_6

PC7 0.1U/50V\_6X

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

R1 PR132 10K/F\_6

R3 PR139 0.4

PR11 0.4/S

PR131 0.4

PR128 255/F\_4

PR130 1K/F\_4

PR5 54.9K/F\_4

PC3 1200P/50V\_4X

PR7 6.81K/F\_4

PC2 1000P/50V\_4X

PR14 18.2K/F\_4

PR140 3.92K/F\_4

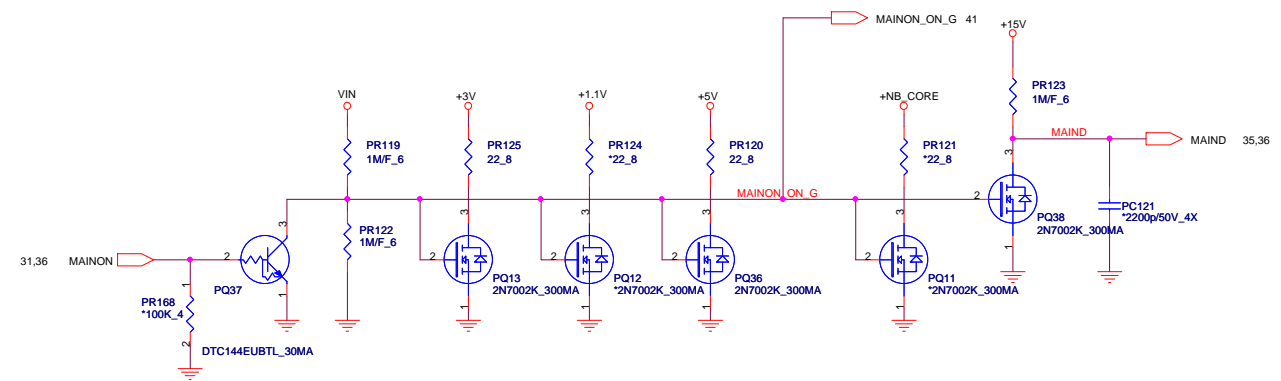
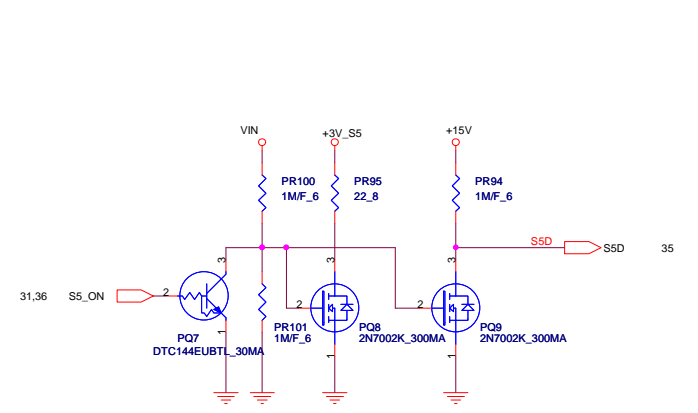
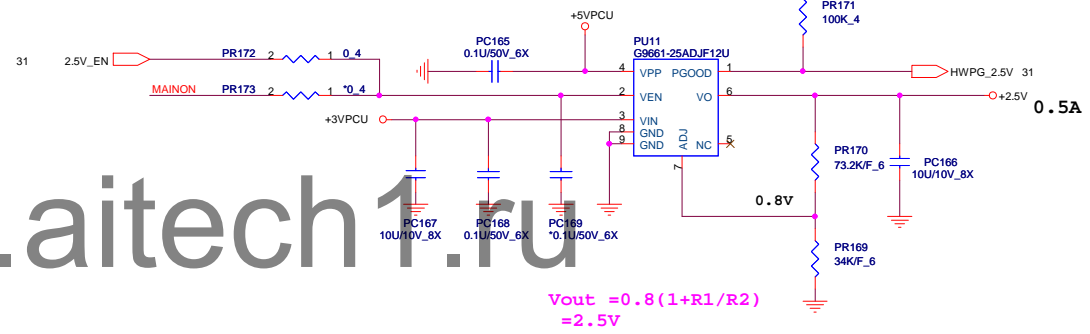
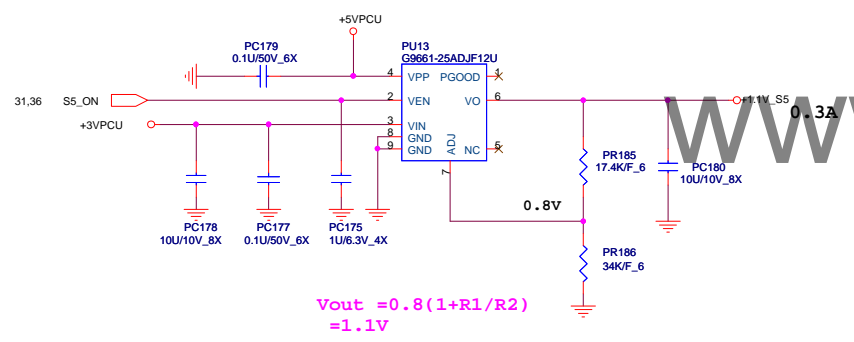
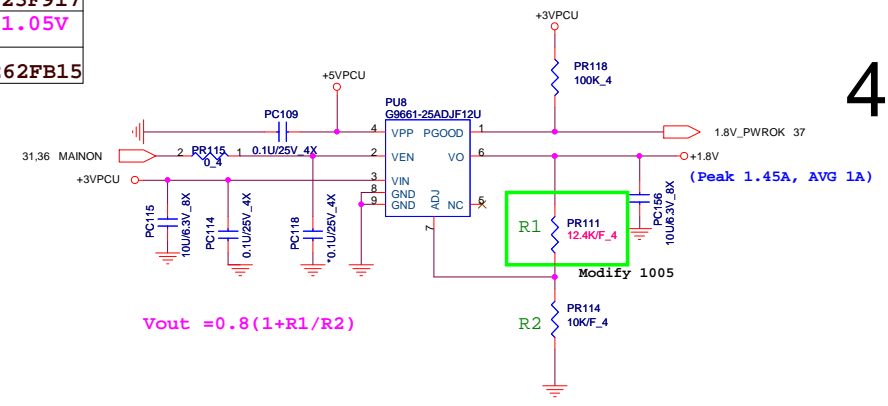
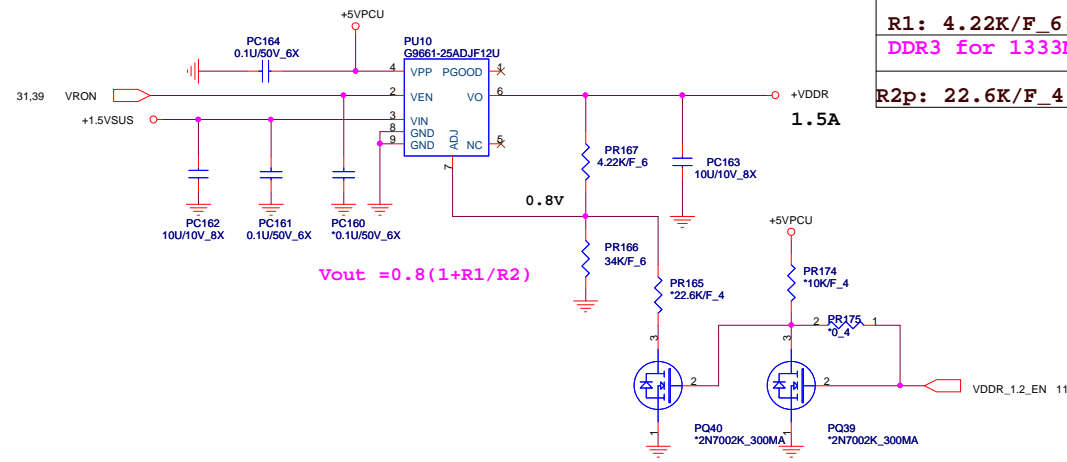
PC16 0.1U/50V\_6X

R2 PR138 1K/F\_4

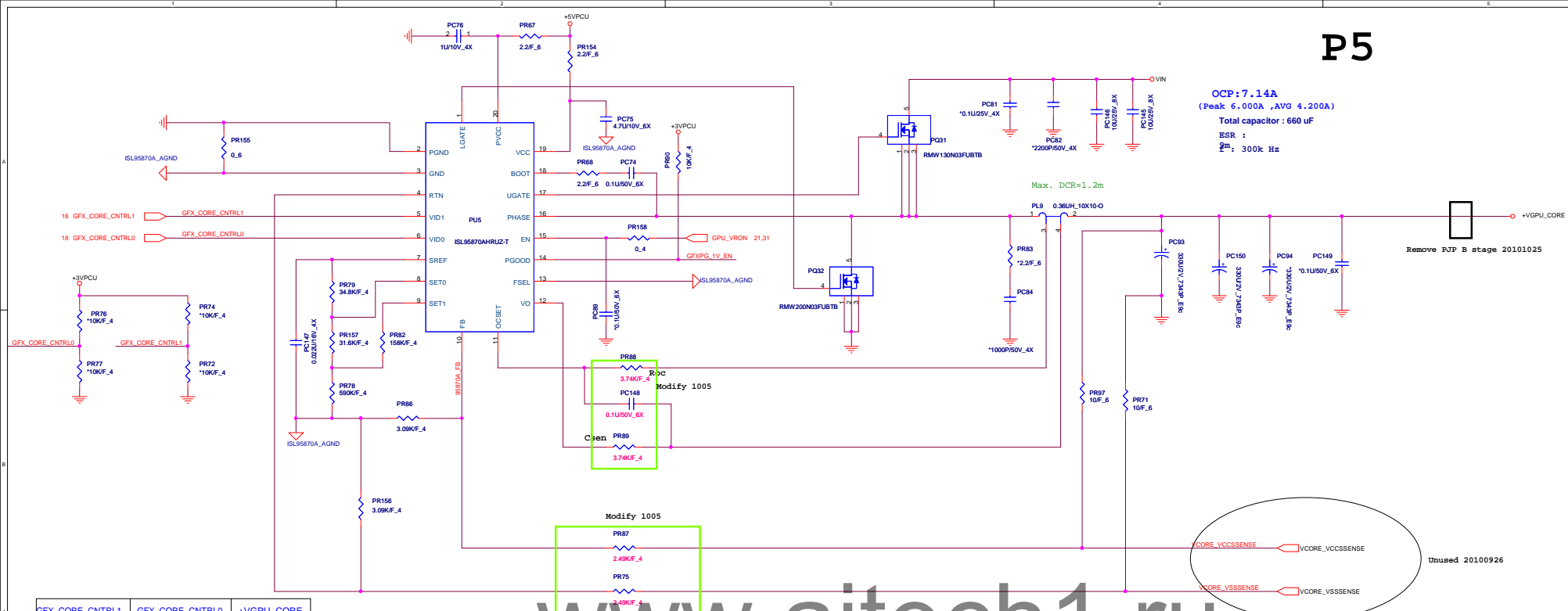
R1 PR132 10K/F\_6

R3 PR139 0.4

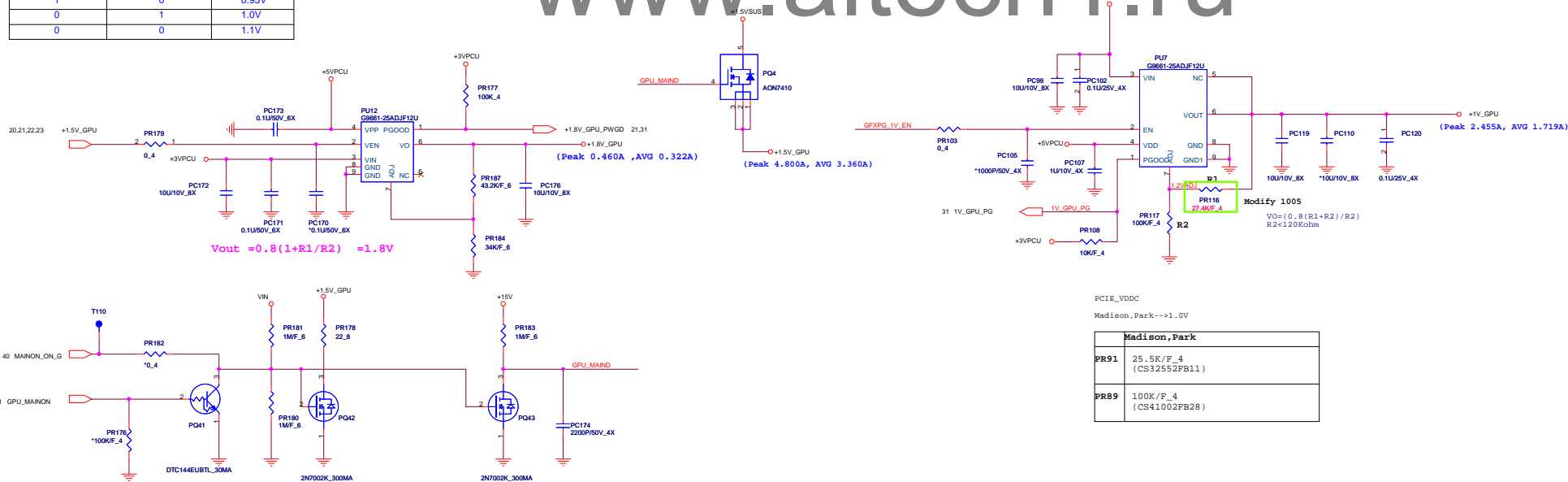
DDR3 for 1066MHZ----0.9V  
 R1: 4.22K/F\_6: CS24223F917  
 DDR3 for 1333MHZ----1.05V  
 R2p: 22.6K/F\_4: CS32262FB15



P5



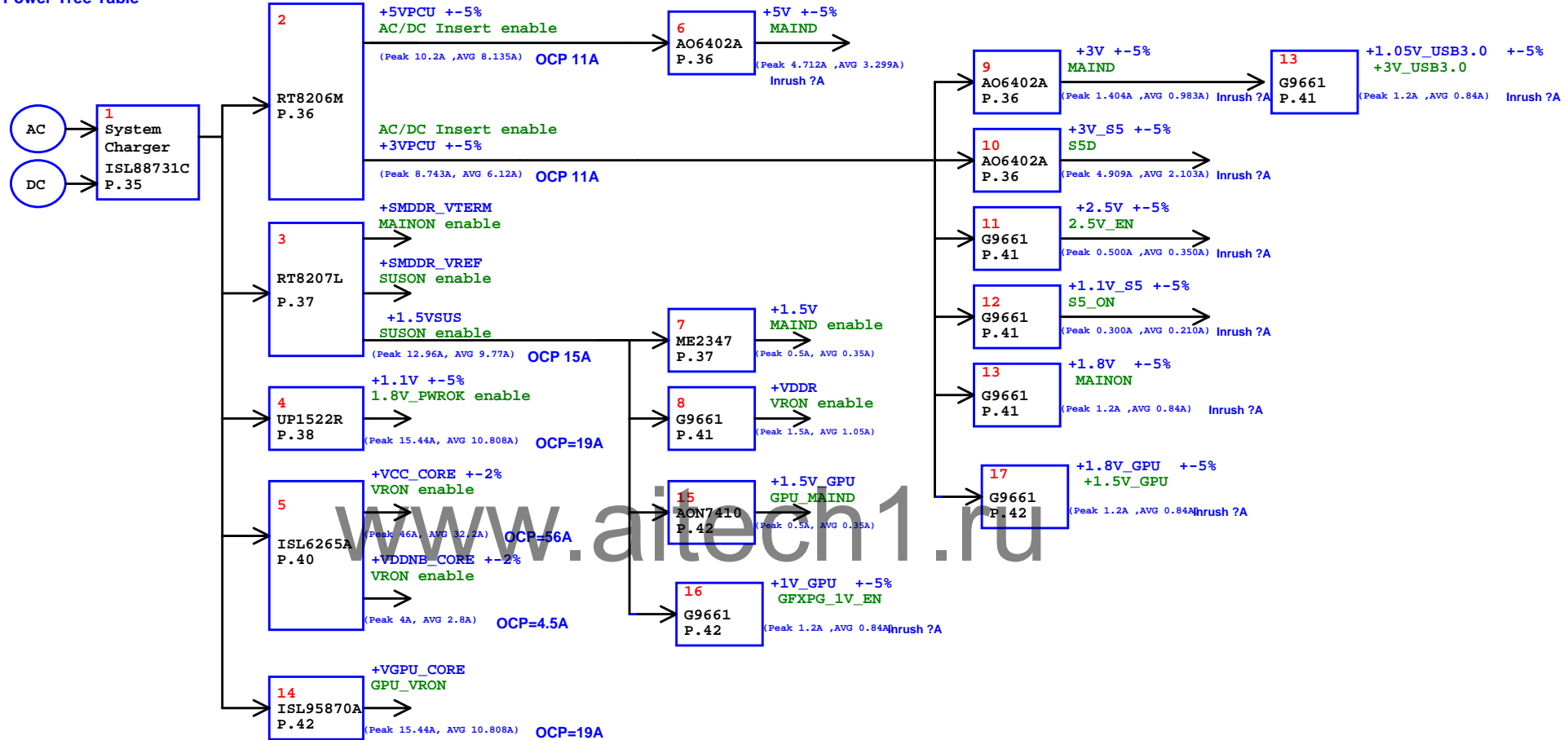
GFX_CORE_CNTRL1	GFX_CORE_CNTRL0	+VGPU_CORE
1	1	0.9V
1	0	0.95V
0	1	1.0V
0	0	1.1V

[illegible]

	<b>Madison, Park</b>
<b>PR91</b>	25.5K/F_4 (CS32552FB11)
<b>PR89</b>	100K/F_4 (CS41002FB28)



Power Tree Table



Power Distribution List

Power	Distribution



Quanta Computer Inc.

PROJECT : TE3

Size	Document Number	Rev
Custom NB4	Power Tree Table	1A
Date:	Wednesday, March 02, 2011	Sheet 42 of 42